A MULTI-MICROPROCESSOR BASED DISTANCE RELAY: DESIGN REQUIREMENTS AND IMPLEMENTATION CHARACTERISTICS

M. Kezunovic, S. Kreso and O. Petrovic

Energoinvest Company, Institute for Control and Computer Sciences, Sarajevo, Yugoslavia

Abstract. This paper describes a Multi-microprocessor Based Distance Relay implementation. Design requirements are outlined first. Detailed discussion of system, maintenance and testing, interface and cost/performance requirements is given. Second part of the paper provides an overview of the implementation characteristics. System architecture, hardware, software and algorithm issues are presented. Finally, a conclusion is drawn related to the major advantages of the design as well as to the future testing and evaluation procedures.

Keywords. Digital computer applications; microprocessors; power system control; protective relaying; digital distance relay.

INTRODUCTION

Application of microprocessors to the area of Electric Power System Control, Protection and Analysis was developing as a research activity during the past ten years (Nguyen, Kezunovic, Dy-Liacco, 1984). During this time period number of microprocessor-based devices and systems were developed and tested in both laboratory and substation enviroments. Some of these devices and systems did appear on the world market in the past couple of years, but a full expansion of this market is expected in the near future.

This paper is concerned with implementation of a distance relaying function using LSI technology. A number of attempts were made arround the world to develope microprocessor-based distance relays and a great variety of the solutions were reported so far (Kezunovic, Kreso, 1984). However, a close look at the characteristics of those solutions shows that there are as many different implementation approaches as there are different solutions. It should be also noted that there are very few commercially available distance relays on the world market and it is expected that final evaluation of the numerious solutions mentioned will actually be driven by the future market expansion.

Major aim of this paper is to discuss basic characteristics of a Multi-microprocessor Based Distance Relay developed for high voltage, medium lenght transmission line protection. Some specific design requirements are discussed first. Characteristics of the solution are presented next. Conclusions are related to the major advantages of the design as well as to the future testing and evaluation procedures. List of references is given at the end.

It should be noted that the Distance Relay presented in this paper is a part of an Ingrated Control and Protection System development and some discussions in the paper are related to this problem as well.

DESIGN REQUIREMENTS

Discussion of the design requirements is related to the specific requirements which are generated by the capabilities of the microprocessor technology. Some standard protective relaying system requirements which are independent from the technology used are not discussed but just briefly mentioned.

Protective Relaying System Requirements

The basic requirements are that relay is to protect medium lenght (order of loo km), high voltage (up to 4oo KV) transmission lines with single and parallel configurations. The relay should also be capable to interface to Automatic Reclosing, Out-of-step and Pilot Relaying modules which are external to the relay. Relay characteristic should be quadrilateral as given in Fig. 1.

Regarding relay operating performance, it should react in Zone 1 with speed in the range of lo-loo ms depending on the type and location of the fault. Relay accuracy should be optimized considering the three major signal processing steps: signal sampling and A/D conversion, line parameter calculation (selection of algorithms), transmission line model presentation (Kezunovic, Perunicic, 1984). Relay should also be selective for specific situations such as close-in faults, voltage collapse, propagating faults.

Maintenance and Testing Requirements

Use of the microprocessor technology brings some specific requirements regarding maintenance and testing. An example is a self-testing requirement which should enable operator to identify faults in the relay hardware. Further more, the relay should be designed to enable exchange-of-modules repair strategy which should decrease MTTR (Mean Time To Repair) system time and hence improve availability performance. Another specific requirement is that relay is

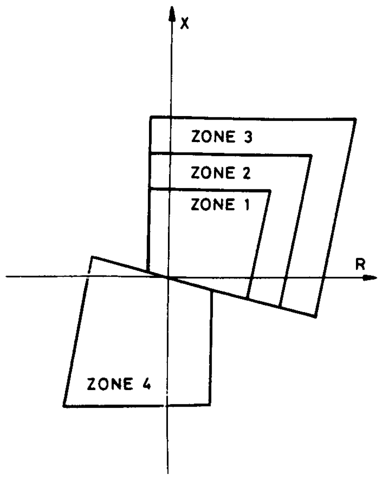

Fig. 1. Relay characteristic

capable of storing intermediate data and parameters for the relay testing purposes. Yet another requirement is capability of auto-calibration and auto-correction for the A/D conversion circuitry which is error prone depending on the temperature changes.

Operator Interface Requirements

Having in mind use of the microprocessor technology, relay operator interface requirements include: classical operator panel, serial link interface, interface to the higher levels in an Integrated Control and Protection System.

Classical interface. Relay should be equiped with a classical operator interface which is implemented using some analog manipulating elements for adjusting relay settings. Signaling elements should be classical lamp indicators. It should be noted that some information related to the relay testing and maintenance should also be exchanged through the classical panel. A care should be paid to disposition of the manipulating elements and indicators so that they correspond to disposition on the classical relays even though the actual way of connecting to the microprocessor-based boards will be different comparing to the classical relays.

Serial link interface. Relay should provide a serial link interface and there should be support for a CRT or a special keyboard interface. This interface should enable relay settings manipulation so that an option is available that relay can be set using this interface only. Further more, a software capability should be implemented so that operator can display on a CRT appropriate intermediate data and parameter values. This would enable presentation to the operator of the internal relay settings as well as the calculated intermediate values needed for the relay development, factory and switchyard testing.

Integrated system interface. This relay should be designed as a subsystem of an Integrated Control and Protection System (Kezunovic, 1985). This requirement asks for implementation of an interface to the higher levels of the Integrated System, where overall Operator System Interface is provided. A requirement is also that row samles, intermediate calculated values and parameters should be transferred through the higher level interface from the relay, and relay settings and operator requests to the relay through the same interface. This interface should also enable exchange of the enabling and blocking signals among all of the subsystems within the Integrated System.

Cost/performance Requirements

The main requirement in this respect is that the microprocessor-based relay design be better or comparable to the solid-state relay design. However, it is evident that the use of microprocessors brings some performance improvements comparing to the solutions based on the previous technologies. A question arises then related to the acceptable cost increase associated with the mentioned performance improvements. It is belived that only the market needs will provide final specification of the cost/performance requirements and therefore close evaluation of the market needs is necessary before such a design is defined and finally offered.

CHARACTERISTICS OF THE SOLUTION

Further discussion is related to the description of the major characteristics of the solution such as: system architecture, hardware, software and algorithms.

Relay Architecture

Analog Input Board (AIB). An outline of the AIB architecture is given in Fig. 2. It can be noted that this is a special purpose microcomputer board designed arround an 8-bit microprocessor and associated digital and analog circuitry (Kezunovic, Kreso, Sarajlic, 1984). It consists of one A/D converter with eight multiplexed inputs. Those inputs correspond to four current and four voltage signals comming from the instrument transformers placed in the switchyard.Mentioned signals are converted by the A/D circuitry and stored in the dual ported memory. Further communications with the main processing board are performed via the MULTIBUS.

Microprocessor Distance Relay (MICRODIR). Atchitecture of the MICRODIR is given in Fig. 3. It should be noted that this is a multiprocessor architecture consisting of three microcomputer boards. One board is the AIB, other board is the main processing board which accomodates an 8086 16-bit processor and an 8087 numeric processor, and the third board is the ETHERNET Controller. MICRODIR is interfaced to the switchyard through the AIB, to the Integrated System via an ETHERNET Controller, to the external equipement (OOS, Pilot, ARC) via an I/O adapter, and to the operator via serial and parallel ports. Major interprocessor communication is done either over a private processor bus or over the MULTIBUS.

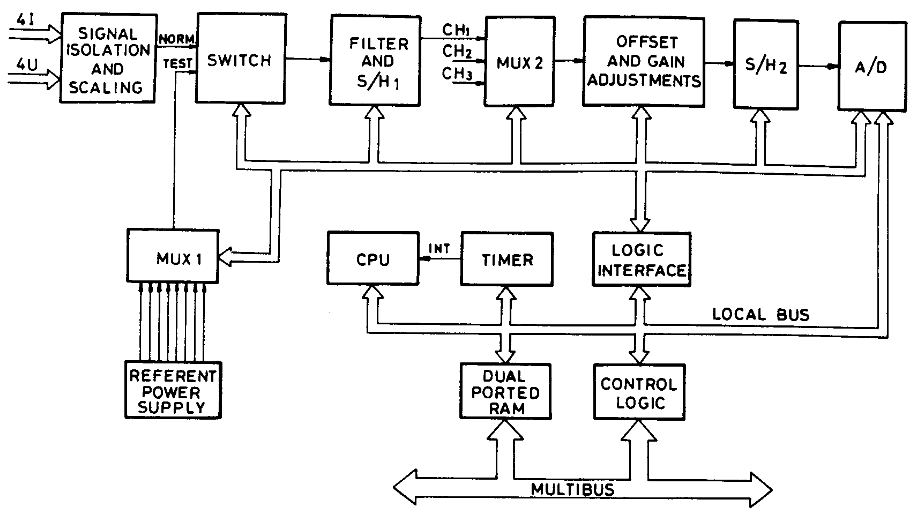

Fig. 2. Analog Input Board architecture

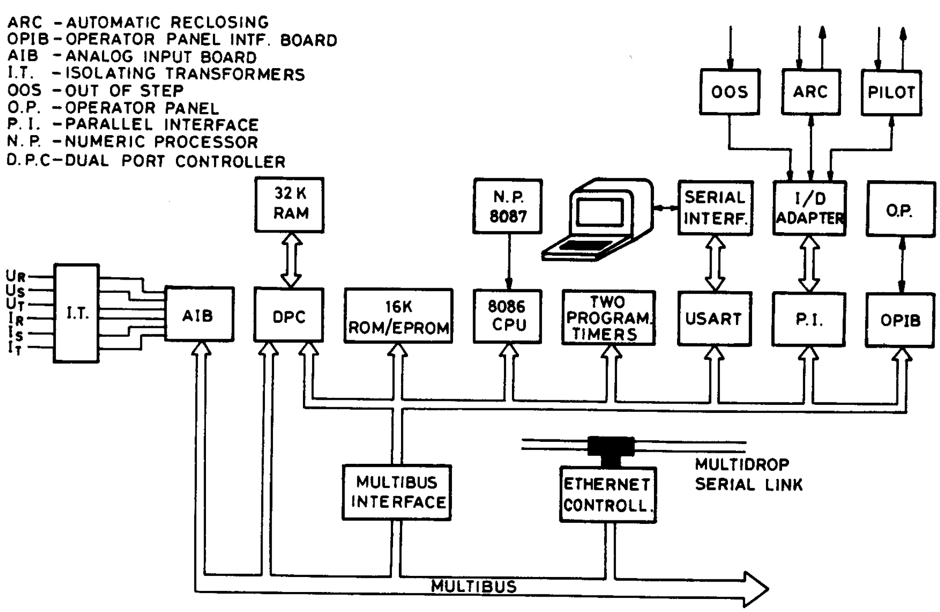

Fig. 3. Microprocessor Distance Relay (MICRODIR) architecture

Integrated System (IS). As it was mentioned in the requirements section of this paper, MICRODIR is a subsystem of the system solution which integrates several devices in an Integrated Control and Protection System. An outline of the IS architecture is given in Fig. 4. As it can be seen, the IS consists of the three devices namely MICRODIR, MICROSTORE and MICROLARTS (Kezunovic, 1985). MICROSTORE is a microprocessor based Transient Recorder and MICROLARTS is a microprocessor based Local Automation device. All of the three subsystems are interconnected over a multidrop serial link. Also, a system operator interface device is included which provides local and/or remote operator interface. This device is also connected to the multidrop serial link and hence represents a system interface for the MICRODIR as well. Multidrop serial interface (MSI) is implemented using an ETHERNET Controller.

Relay Hardware

Analog Input Board. This is a MULTIBUS compatible custom designed board. This is quite a complex hrdware solution which contains capabilities to perform self-checking, auto calibration, and gain and offset correction. It also contains an 8-bit microprocessor to control an A/D converter circuitry as well as to perform mentioned testing functions. It should be noted that this complex solution was needed because the analog input circutry is quite sensitive to the temperature changes and yet it can be shown that accuracy of the overall algorithm is quite dependent on the accuracy of the A/D signal processing circuitry. Further more, in order to optimize overall relay processing hardware design, it was conceived that some of the data processing for relaying purposes can be done using this board. Finally, the design is quite flexible and programmable since it was produced under wider Integrated System requirements so that it can be used for some other subsystems within the Integrated System. Detailed discussion of the AIB hardware can be found in Kezunovic, Kreso, Sarajlic, 1984.

MICRODIR. The relay is designed arround INTEL family of microprocessor chips and boards. The main processing board is an OEM INTEL 86/14 board with an iSBC 337 multiboard used. ETHERNET Controller is also an OEM product. An ETHERNET board which needs a separate CPU board as a controller is used at present, but future design should use an inteligent single board ETHERNET controller.

Other MICRODIR boards are custom designed. Those include the AIB, the operator panel interface board, the I/O adapter board and the isolating transformer board. Custom designed are the power supply boards as well.

Relay Software

AIB software. flow diagram for the AIB software is given in Fig. 5. This software consists of two subroutines. One is the initial correction subroutine which calculates initial correction factors for zero input and offset values. Another subroutine is used for actual A/D conversion pro-

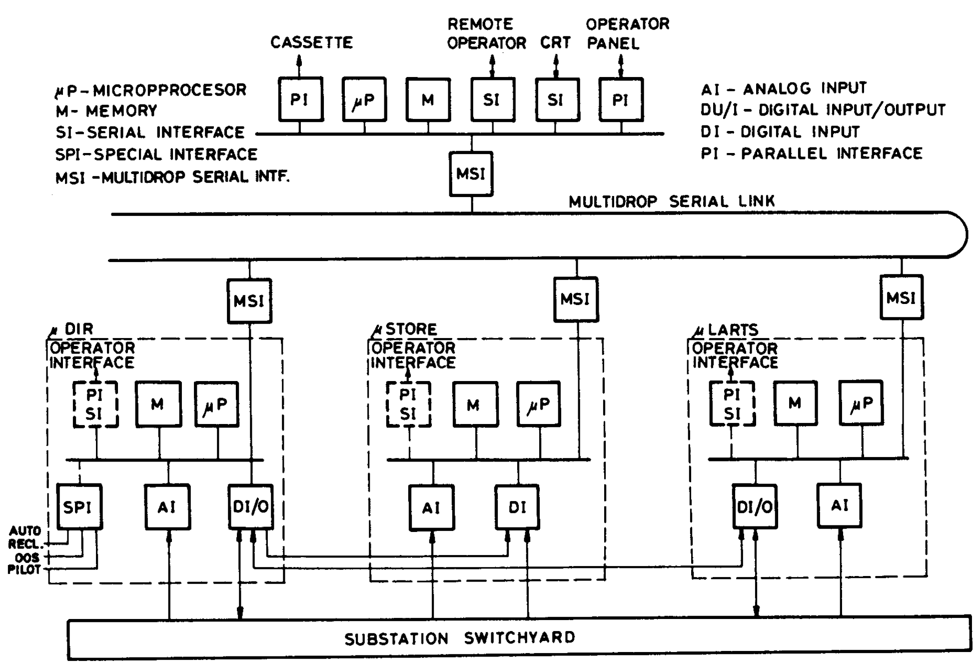

Fig. 4. Integrated system architecture

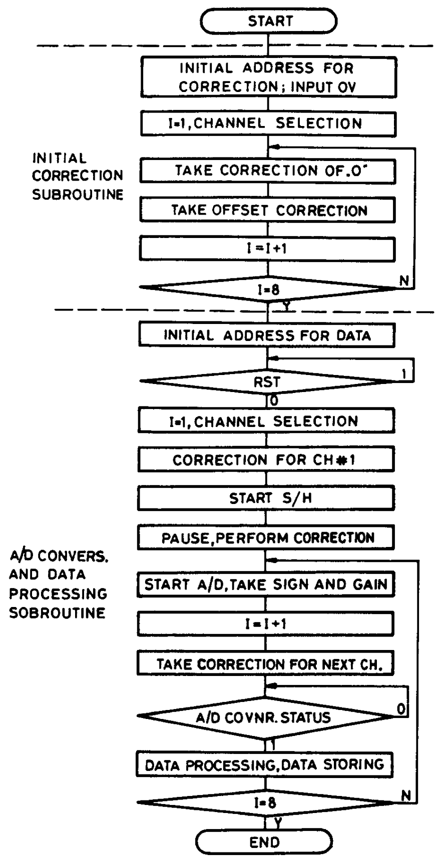

Fig. 5. AIB software

cessing. It can be seen that the correction factors from the first subroutine are used later on for the corrections undertaken in the second subroutine. It can be also noticed that in the second subroutine a parallel action is taken i.e. while A/D conversion is in progress on channel 1, corrections are made on channel 2. This parallel action enables the best utilization of the processor time.

The AIB software discussed is executed during ecch sample time. However, there is some additional software which is executed only during the star-up time as well as during the testing and calibration procedures.

MICRODIR application software. Flow diagram for the MICRODIR application software is given in Fig. 6. It can be seen that software consists of a start-up and testing part and a fault processing part. First part is executed at the power-on time when the relay is put in service. Second part is executed all the time i.e. an iteration is made each time the samples are taken.

Start-up and testing part are used to initialize relay hardware as well as to perform detailed testing of the overall relay hardware. This software is also executed whenever a reset of the relay is initiated.

Fault processing part consists of fault detection, fault classification and fault verification procedures. Fault detection is executed each time the new samples are taken and serves as a starting procedure for rest of the algorithm. When a detection flag is set then the fault classification procedure is initiated. This procedure determines type of the fault and accordingly selects V,I pair for further processing. The further processing is related to calculation of R and X values which are then compared against a relay characteristic of a quadrilateral form. If the calculated values are inside the zones, a tripping action is initiated.

Special routines, not shown on the diagram, are used to reconstruct the voltage samples in the case of a voltage collapse. Also, a routine is available to perform resistance correction in the case of ground faults.

Due to the stringent speed-of-execution requirements application software is implemented using assembler programming language. Further more, special care is paid to the optimal assembler code design regarding full use of parallel processing on processors 8o86 and 8o87. Finally, structured and modular code design is developed to support software testing and maintenance.

Software for system services. This software consists of maintenace and testing part and a part which supports operation of the MICRODIR and related ETHERNET controller.

Maintenance and testing software includes several routines. One routine is related to the self-checking tests which are executed during the relay operation. Yet another routine is executed during extensive factory or field testing related to relay commissioning or maintenance. There are two options for this routine.

First option of the extensive testing routine is developed for a semi-graphic terminal. A flow diagram of the program DISPLAY is given in Fig. 7. It consists of the static display part which gives a format of the dynamic displays. Dynamic display part calculates points of the impedance locus as well as other intermediate values and parameters. Points of the impedance locus are drawn on the impedance diagram and rest of the values are put in the related tables.

Another option is developed for an alphanumeric CRT. Flow diagram of the program DISPK is given in Fig. 8. This program is oriented toward presenting intermediate values and parameters generated and/or set in the modules of the application software. It should be noted that special software is developed to collect real-time data to be displayed by this program. Displays are organized in two pages and there is a hierarchical procedure for initiation of the displays. Logic is established which enables presentation of only those displays which correspond to the modules executed during the last iteration of the application software. It is also possible to scroll through the displays and pages in either direction.

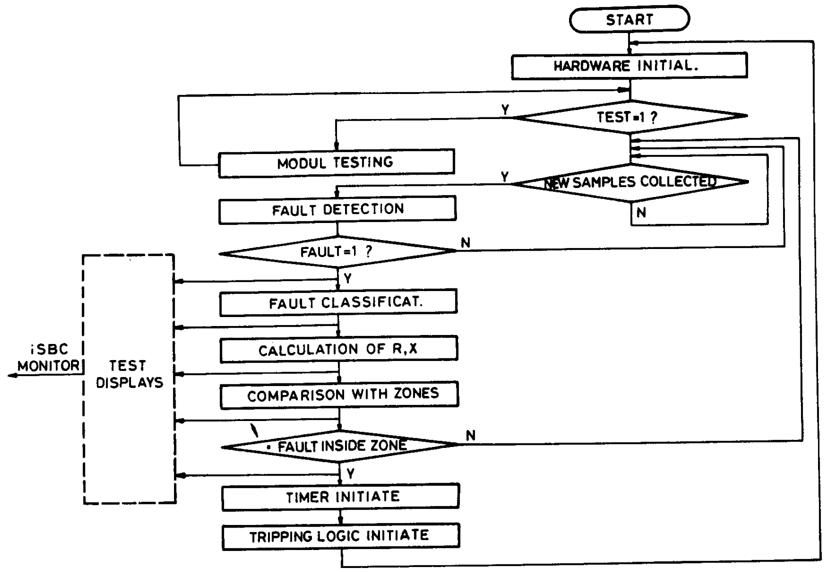

Fig. 6. MICRODIR application software

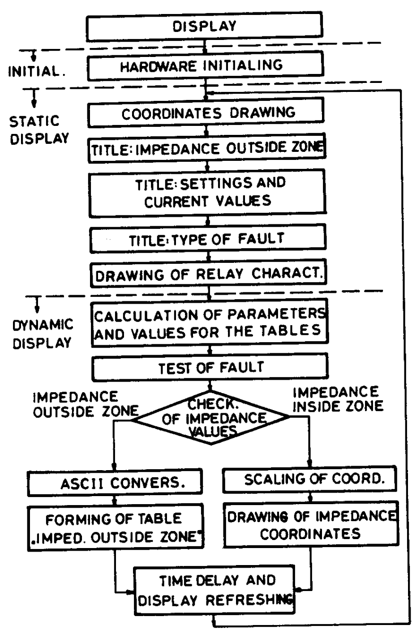

Fig. 7. Display on a semi-graphic terminal

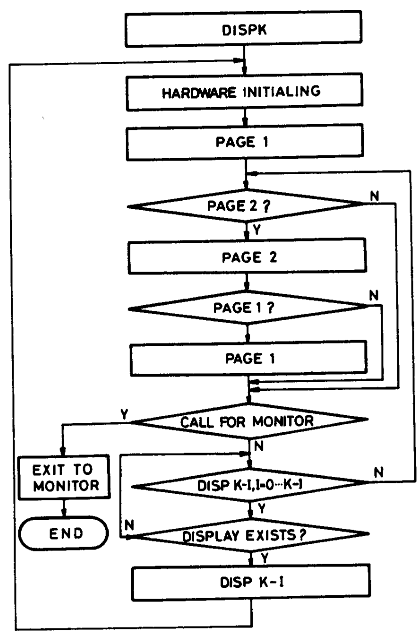

Fig. 8. Display on a CRT terminal

Relay Algorithms

Algorithms selected in the MICRODIR design are some modification of the already known algorithms. However, two algorithms studies are undertaken to investigate problem of algorithms in more detailes. Those studies are in the final stage of completion and the final MICRODIR algorithm decision might be affected by the outcome of those two studies.

Algorithms implemented. As it was mentioned in the software section, overall algorithm consists of the fault detection, fault classification and fault verification procedures. Both fault detection and fault classification procedures are using samples and amplitude values to make a decision (Gilcrest, Rockefeller, Udren, 1972; Rockefeller, Udren, 1972). Detection is performed by comparing samples of a waveform at the moment of a fault with the samples of the same waveform a cycle ago. A detection criterion is also based on the amplitude values overreaching certain treshold. Amplitude values are calculated using a fast 3-sample algorithm (Gilbert, Shovlin, 1975).

Fault classification is also performed based on both samples and amplitudes. An outcome of this procedure is a V,I pair used for the fault verification procedure. It should be noted that there are two classification procedures, one based on voltage and one based on current signals.

Fault verification algorithm is based on solution of a differential equation which provides algorithms to calculate parameters R and X (McInnes, Morrison, 1971). Those values are further used for fault verification and tripping decision.

Algorithms studies. The two algorithms studies are performed in parallel to the implementation activity and major goal is to perform evaluation of the existing algorithms as well as to derive a Generalized Algorithm Form.

Evaluation study should provide a classification scheme for the algorithms (Kezunovic, Perunicic, Kreso, 1985). It should also give criteria for algorithms rating based on the application conditions as well as on the relay design characteristics.

Study of a Generalized Algorithm Form (Kreso, Kezunovic, 1984) should define a common form to represent all of the algorithms. Certain parameters of the form would be adjustable to take into account specific requirements of the unique properties of some of the algorithms. This study would enable comparison of the various algorithm forms proposed so far in order to define a unique form for number of the similar algorithms.

Results of the two studies should provide required background to fully verify performance of the MICRODIR. Those result would be also used for a new study related to development of an Expert System for engineering design of a new generation of protective relays based on microprocessors. Basic goal would be to develope an Expert System which should provide an optimal relay design given the application conditions of a specific Electric Power System.

CONCLUSIONS

Design of the MICRODIR provides optimal solution to the stringent speed-of-execution requirements using standard hardware and software techniques which results in an acceptable cost/performance characteristic of the product. Preliminary laboratory test results are encouraging and further tests in a High Power Laboratory and a substation will be carried out in the near future. Overall Integrated System testing will be also performed soon

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