Real-Time Digital Simulator for Protective Relay Testing

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Analog power system simulators have been used for a long time in performing relay testing. A number of new transient simulator designs have been introduced in which improved performance and lower cost were the major goals. Using electronic hybrid technology, where both analog and digital components are used, is a promising approach. A typical example of high performance electronic design is a transient real-time simulator developed for protective relay testing by ABB Relay Division in Sweden in the 1980s. However, the cost of building such a design is still out of reach for many utility companies.

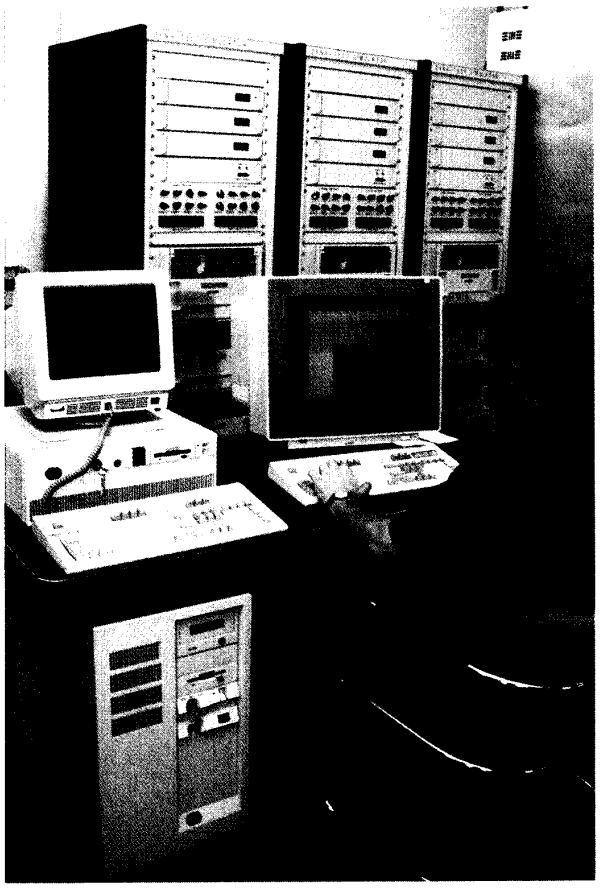
WAPA implemented a new low-cost, high-performance digital simulator design aimed at providing real-time operation while preserving accuracy and flexibility

The most recent approaches are to use digital technology to implement protective relay testing simulators utilizing power system and fault modeling capabilities of electromagnetic transient programs. This approach offers modeling accuracy and user flexibility. First such designs were introduced by GEC Alshom Measurements in England in the early 1980s and by Bonneville Power Administration in the United States in the mid-1980s. The use of these simulators has demonstrated some major advantages in meeting complex relay testing requirements, such as fault studies on series compensated lines. However, the main disadvantage of early digital designs was difficulty in providing any meaningful interaction between the relay and the simulation computer. The numerical techniques implemented in the existing electromagnetic transient programs did not allow for the required real-time switching of system configurations as often needed for fault simulations.

This article describes a new digital simulator design which is aimed at providing the real-time operation not available in the previous designs while preserving the accuracy and the flexibility already demonstrated by the digital implementations. This is achieved by using low-cost commercial hardware and system software as well as custom-designed user interface and real-time application software.

DOE-WAPA Digital Simulator Project

The Western Area Power Administration (WAPA) recognized that real-time testing of protection relays is needed for a full evaluation of different relaying products considered for future use on the WAPA system. In terms of protective relaying, some important sections of the WAPA sys-



The real-time digital simulator design is quite powerful in evaluating protection relays, yet it is affordable for wide-spread utility use.

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tem have introduced several real challenges in deciding which relaying product will best suit the given application. The relaying applications are quite complex, consisting of parallel lines with series capacitor compensation, MOV protection on the capacitors, and a single-pole reclosing scheme.

As a result, WAPA decided to use real-time simulators for future evaluation of the protective relays and the overall relaying schemes. The main requirement was the high accuracy of modeling and the user interface flexibility. However, the main constraint was a requirement for the low cost of implementation. The obvious choice was to utilize digital technology to implement a real-time simulator that will meet the requirements.

A real-time simulator project was initiated by WAPA in 1989. Since there were no real-time digital simulator products offered on the market at that time, WAPA decided to fund Texas A&M University to build such a simulator. A contract was signed in late 1990, and a design approach was specified by late 1991. The simulator was implemented by the end of 1993. Since that time, it was tested and delivered to WAPA in the first quarter of 1994.

Texas A&M University has been involved in studying digital simulator applications for the Electric Power Research Institute (EPRI) under RP 3192-01. Various results from the EPRI study were quite informative in better understanding the general requirements for digital simulator implementation for relay testing. Even though the EPRI study was related to an open-loop digital simulator design, and did not include real-time digital simulator requirements, several outcomes of the EPRI study turned out to be useful for the real-time simulator implementation. In particular, an EPRI design of high accuracy, high power I/O interfaces between the simulator and the relays has proven to be an excellent solution. It has been directly used for the WAPA simulator implementation. Also, results of the EPRI study of transient responses of instrument transformers, in the case of system faults, were quite enlightening when a choice of the instrument transformer modeling detail was made for the WAPA project.

Table 1. Application requirements for relay testing

Application	Requirements
Parallel lines	Three terminal simulator configuration and modeling of coupled R-L branches
Series compensated long lines	Modeling of distributed and frequency dependent parameter lines
MOV and arrester protection	Modeling for short line representation
Close-in and Far-end faults	PI circuit modeling for short line representation
Single-pole auto reclosing	Real-time interaction, modeling of circuit breakers and switches
Different fault cases	Selection of fault type, resistance incidence angle and location
Influence of relaying transformers	Accurate modeling of CCVT and CT transient response
Timing sequence of circuit breakers	Modeling of circuit breaker timing logic

Table 2. Simulator design criteria and implementation requirements

Criteria	Requirements
Software portability	UNIX environment
Application software modifications and upgrades by the user	Extensive system software for program development and debugging
Flexibility in setting up simulations and tests	Graphical user interface software
High precision, high power waveform reconstruction	New design of D/A and power amplifier subsystem
Real-time simulation of transients and faults and real-time simulation of instrument transformer responses	Development of a new real-time application software for network and instrument transformer transient simulation
Frequency response up to 20 kHz	Simulation time step of 50-100 microseconds

Design Requirements and Implementation Approaches

WAPA has defined several application requirements for relay testing that the new simulator design had to meet. A summary of these requirements is given in Table 1.

Besides the application requirements, WAPA placed several criteria for the simulator design approach. This has resulted in some additional implementation requirements listed in Table 2.

As a result of the requirements, the research team was faced with the following major design tasks:

- Selecting a suitable commercial computer hardware and system software architecture for simulator implementation
- Selecting a suitable high precision, high power I/O interface
- Developing new real-time application software for generation of fault transients
- Implementing real-time interaction between digital simulator and I/O subsystem used for interfacing with protective relays under test.

In selecting an appropriate commercially available computer system architecture, the first task was accomplished by running several benchmark programs on a number of different high-performance computer architectures. After an elaborate study was concluded, it was apparent that none of the low-cost, high-performance parallel architectures were suitable for the simulator application. The only remaining choice was to select a distributed computer architecture consisting of several low-cost, high-performance, single-processor computers. Further evaluation led to the choice of IBM RISC 6000 computers in a combination with Sonitech DSP boards.

Table 3. Commercial hardware characteristics

Characteristic	IBM RISC 6000/580	IBM RISC 6000/320	Sonitech DSP Board
Clock frequency	62.5 MHz	25 MHz	40 MHz
Processor type	RISC	RISC	TMS 320 C40
Memory system	64 MB	16MB	2 MB
Bus width	128 bit	64 bit	32 bit

The second task in selecting a high-precision, high-power I/O interface was accomplished by utilizing such a design developed under EPRI project RP 3192-01. This equipment was manufactured, under the EPRI sponsorship, by a commercial vendor.

The task of developing real-time simulation software led to an in-house implementation of an EMTP-like software customized for high-speed execution. A number of new numerical approaches and algorithms were introduced to represent and simulate power system components. Some of the results of this development are already published and further details are being prepared for future publication in the IEEE Transactions.

Finally, implementation of the real-time interaction between the digital simulator and the I/O interface was carried out by developing special I/O cards. Printed circuit board (PCB) layouts for these PCBs were done by Texas A&M University, while the boards were produced by a commercial PCB manufacturer. Component mounting and board testing has also been performed by Texas A&M University.

Digital Simulator Characteristics

Simulator architecture is shown in Figure 1. It is a distributed system architecture with two IBM RISC computers and two Sonitech DSP boards, each dedicated to a particular processing task. The task allocation is such that the user interface interaction is performed offline. The real-time interaction between the power system network, instrument transformer, and circuit breaker simulation is achieved by a careful coordination among tasks executed on IBM RISC 6000/580 and Sonitech DSP computers. Furthermore, real-time interaction between the simulator and the relay under test is implemented through the high-precision, high-power interface that outputs analog waveforms and contacts to the relays, and takes the trip signals from the relays back into the simulator.

The hardware and system software are commercially available products. The only exceptions are some communication support software routines written as device drives for the three I/O boards developed by Texas A&M University. In Figure 1, these boards are identified as the I/O board blocks. The I/O board block between the IBM RISC 6000/580 and the Sonitech DSP computers consists of two interface boards, each connecting the respective computers to the parallel communication link between them. The I/O block connecting Sonitech DSP boards to the high-precision, high-power interface contains one interface board that converts parallel data coming from the DSP board into a serial communication format used to send data to the high-power interface. Some major performance characteristics of the commercial computer hardware used for the simulator implementation are shown in Table 3.

The high precision, high power I/O interface is packaged in a 19-inch cabinet housing D/A conversion boards, as well as up to four current amplifiers and four voltage amplifiers. The D/A boards and the voltage amplifiers were designed by Texas A&M University, while the current amplifiers are selected from a standard product line of TECHRON, a division of Crown International. A cabinet prototype was assembled and extensively tested by Texas A&M University, after which a commercial version of three cabinets was manufactured and used in the WAPA simulator configuration. Some

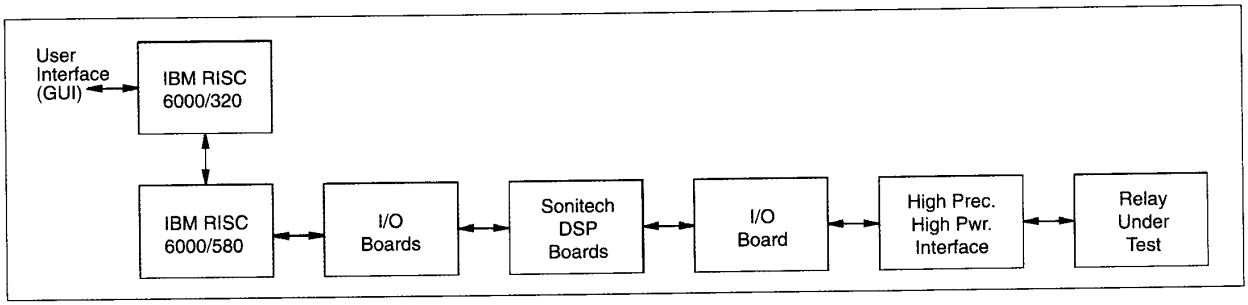

Figure 1. Real-time digital simulator architecture

basic characteristics of this design are shown in Table 4.

Table 4. Basic characteristics of the I/O cabinet design

Item	Specification
Reproduced bits	16
Sample rate	Fs = 3.2 to 25 kHz
Output impedance	Voltage channels: < 1 ohm; current channels: > 500 ohms, dc to 1 kHz
Analog bandwidth	dc to 0.45 fs
Output signal range	Voltage channels: > 320 V_{peak} and 0.2 A_{peak}; current channels: > 160 A_{peak} and 100 V_{peak}
Analog channels	12 voltage (3 sets of 4) and 12 current (3 sets of 4)
Digital channels	48 input (3 sets of 16) and 48 output (3 sets of 16)
Channel skew	< 1 microsecond

Application software has been developed by Texas A&M University, and customized for real-time application. A block diagram of the application software is shown in Figure 2.

The GUI block designates an elaborate graphical user interface developed to enable the operator to interact with the rest of the application software in a very simple and straight forward way. For example, to develop network simulation models, operators need only to use a mouse to move predefined icons of network components to the drawing part of the screen. By a simple connection of these components, the network model is built. Component parameters are entered in a menu-driven screen, which is obtained with a click of the mouse on a given component. Furthermore, the faults are selected by connecting an icon representing a given fault type. The appearance of the GUI screen is shown in Figure 3. The GUI software resides on the IBM RISC 6000/320 computer.

The RTS block represents the real-time system. This application software package consists of a real-time transient network simulation module and a module for real-time interaction with the DSP boards. The transient simulation module enables changes of the network topology in real-time as a trip signal from the relay is received. The component models supported by this module are:

- Uncoupled R, L, C, and R-L branches
- Coupled R-L branches
- Pi circuits for short lines representation
- Constant parameter overhead transmission lines
- Transmission lines with frequency dependent parameters
- Voltage sources
- Faults
- Relays
- Switches and circuit breakers
- Series capacitors with MOV protection
- Surge arresters
- Instrument transformers (CTs and CCVTs).

It is important to recognize that this software module employs some of the most advanced numerical approaches and algorithms that make it possible to run real-time network simulation on a single-processor computer. The RTS resides on the IBM RISC 6000/580 computer.

The SM&CBM block consists of the system manager (SM) and circuit breaker modeling (CBM) software modules. These modules reside on one out of the four DSP chips available on the two DSP boards. The SM module coordinates real-time interaction related to data trans-

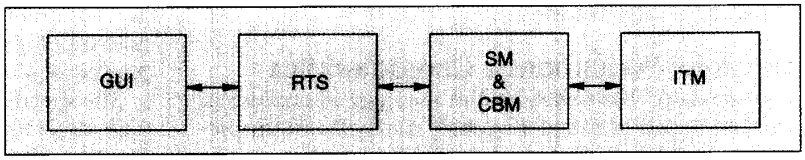

Figure 2. Application software.

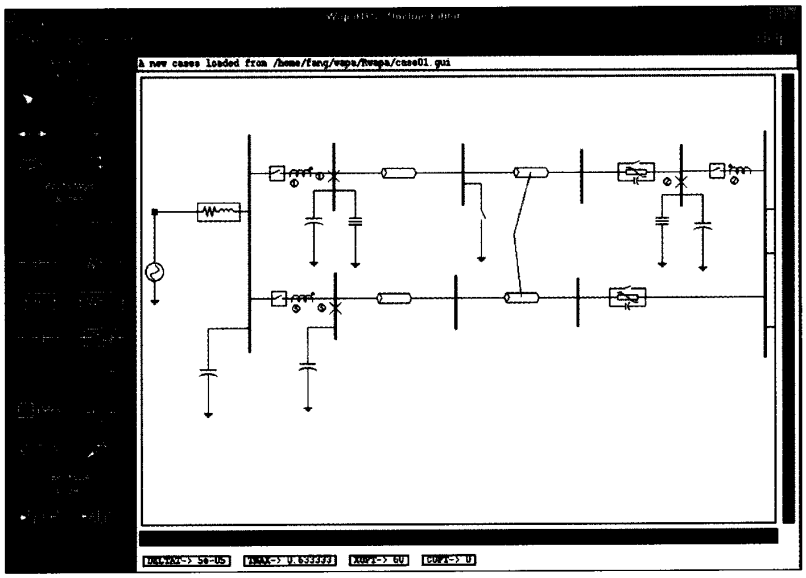

Figure 3. Sample GUI screen

fers between RISC 580 computer and other DSP chips. This includes the transfer of samples of waveforms and contacts going out of the RISC 580 computer to the relay interfaces, and contacts returning from the relay interfaces through the DSP chips. The CBM module incorporates a full timing logic of a breaker. Each of the relay trip signals goes through this timing logic before the signals are transferred to the RTS module, eventually causing a change in the network topology.

The instrument transformer model (ITM) block is related to the detailed models. This block consists of three sets of modules, each residing on one of the remaining DSP chips. Each of these modules comprises three CCVT models and three CT models, which are executed for each time step. This approach to the ITM software implementation enables full modeling of up to 18 instrument transformers in a three-terminal protective relay testing configuration.

The application software also includes a number of support routines that enable real-time interaction between all packages. All of the software residing on the IBM RISC machines is written in C language. This software is portable to any UNIX-like environment, and, in particular, it is upward upgradable for any new set of IBM machines that may become available in the future. The software written for the DSP chips is in the assembly language and can run on any future upgrades of the TI C40 chip-based boards.

Simulator Performance Characteristics

The simulator was tested for the accuracy of producing and the speed of calculating fault transients. Both the accuracy and the speed were evaluated using two models of the WAPA system section, one of which is a simplified version of the other. Figure 4 shows one-line diagrams of the two network models.

Table 5. Comparison of the speed of new IBM machines

Features	580	58H	590
Clock rate	62.5 MHz	55 MHz	66 MHz
Benchmarks			
SPEC int92	73.3	97.6	117.0
SPEC fp92	134.6	203.9	242.4
MFLOPs	38.1	101.1	130.4

The accuracy of simulation was checked by comparing EMTP and RTS waveforms for the same fault event. In most cases, the comparisons have shown very little difference. However, in some cases where the RTS models and algorithms are different from the ones used in EMTP, the waveforms were not the same. Fortunately, these differences do not seem to have an appreciable impact on the current and voltages the relays see.

Typical waveforms from EMTP and RTS for the same fault case are shown in Figure 5. The event shown in the figure represents phase B-to-ground fault with fault incidence angle of 0 degrees and fault resistance of 10 ohms. The fault is located at 50 percent of the line as indicated in Figure 4a. The waveforms are simulated with a 50-microsecond time step at the Glen Canyon end of the line. The real-time switching sequence includes single-pole tripping on phase B, reclosing, and three pole tripping on all phases.

The speed of computation was evaluated based on the time step required to carry out simulations in real-time. The time step depends on many things, such as network complexity, number of MOV and circuit breaker operations, type of fault, and models used for representation of network components. Most of the simulations using the *reduced* WAPA case were carried out with the time step between 50 and 100 microseconds. The *full* WAPA cases required time steps over 100 microseconds. This performance was considered quite acceptable, since it met all of the major design requirements set by WAPA.

It is also important to recognize that the speed of computation is directly dependent on the performance of the IBM RISC 6000/580 machine. In the mean time, IBM has introduced two updates of the RISC 6000 series. Table 5 compares the speed improvements between the machine used in the WAPA

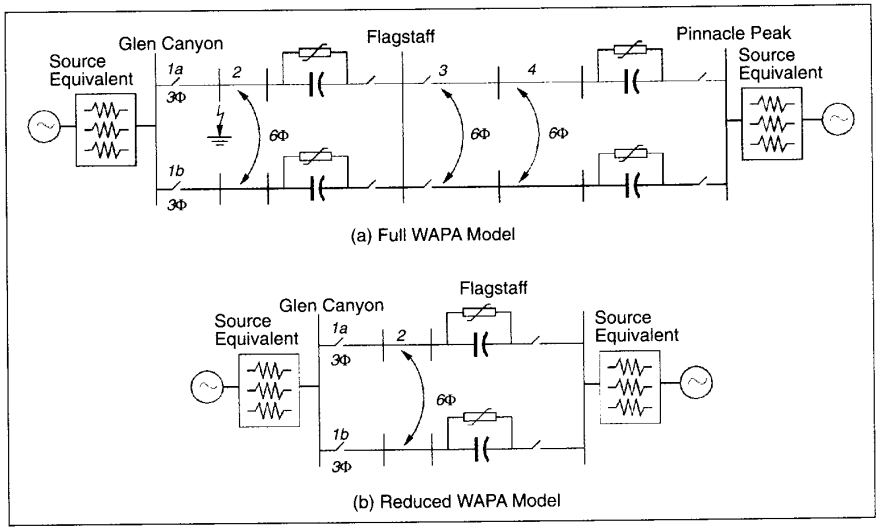

Figure 4. Full and reduced WAPA network models

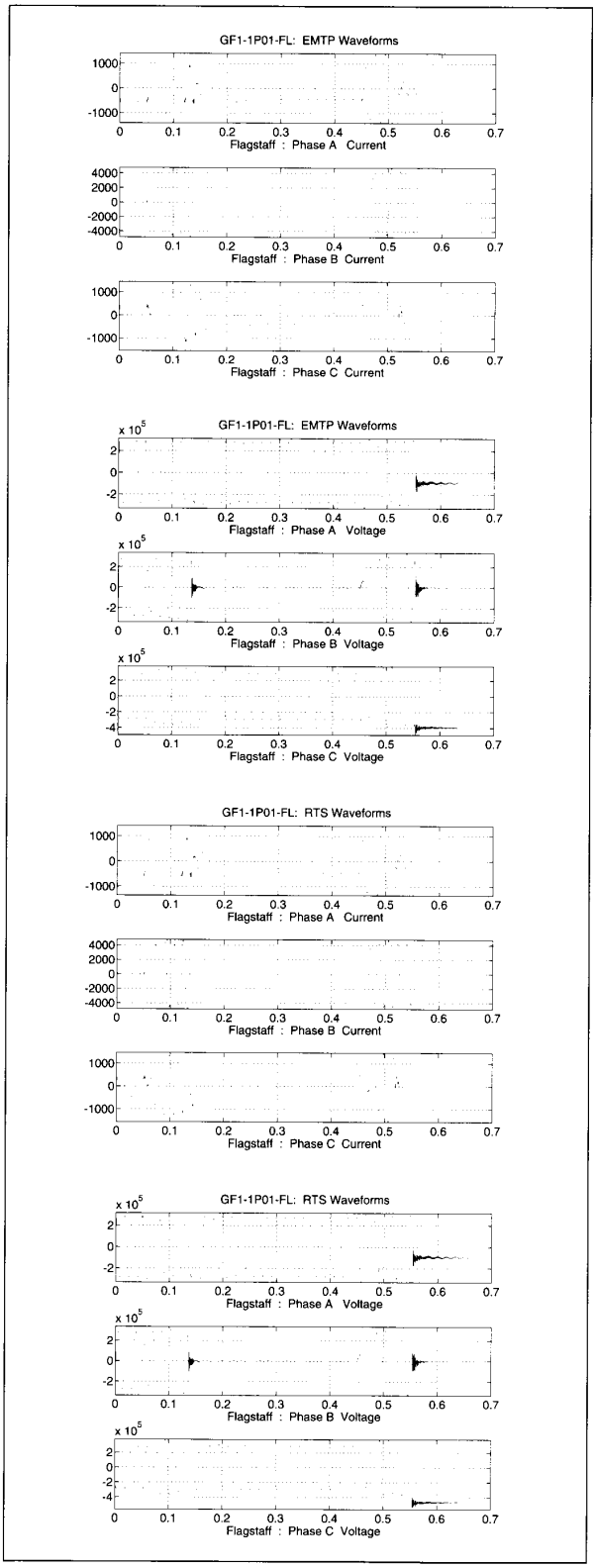

Figure 5. Comparison of EMTP and RTS waveforms

design and the new machines. It is obvious that if the latest machine is used, computational speed performance will improve at least 40 percent over what is achieved in the present design.

Experience and Results

The experience and the results of the WAPA simulator project indicate the following:

- It is possible to design a low-cost, high-performance simulator for relay testing by using advanced digital technology.
- The digital simulator design can offer both improved accuracy and enhanced flexibility while the real-time operation is maintained.
- Simulation time steps between 50 and 100 microseconds are feasible, with an obvious trend of improvements in the future.
- The real-time digital simulator design is quite powerful in evaluating protection relays, yet it is affordable for a wide-spread utility use.

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For Further Reading

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Biographies

M. Kezunovic received his Dipl. Ing. degree from the University of Sarajevo, Yugoslavia, the MS and PhD degrees from the University of Kansas, all in electrical engineering in 1974, 1977, and 1980, respectively. He has been with Texas A&M University since 1987. He is an IEEE senior member, member of the IEEE PES Power System Relaying Committee, and chair of the Working Group on Intelligent System Applications in Protection Engineering and the Working Group on Digital Simulators for Relay Testing. He is a registered professional engineer in Texas.

S.M. McKenna was born in Spokane, Washington in 1951. He earned his BS degree from the Colorado School of Mines in 1978. He joined the Western Area Power Administration in September 1980. McKenna is currently in the Substation Control Branch, where he is involved in control system design for advanced technology devices, protective relaying application and testing, and power system testing. He is a registered professional engineer in Colorado.