DYNA-TEST Simulator for Relay Testing Part II: Performance Evaluation *

M. Kezunović, A. Abur, Lj. Kojović
V. Skendžić, H. Singh
Texas A&M University

C. W. Fromen, D. R. Sevcik
Houston Lighting & Power Company

Abstract - *This paper illustrates evaluation steps undertaken in the analysis of the DYNA-TEST Simulator performance. The evaluation assumes comparison of the simulator output waveforms obtained using simulated data with the reference waveforms obtained through recording of an actual fault event. Tests are done using specific utility data. Particular attention is given to the system and instrument transformer modeling as well as to the D/A signal reconstruction subsystem characteristics.*

Keywords: Power system modeling, EMTP, CT, and CVT modeling, relay testing.

INTRODUCTION

DYNA-TEST Simulator is a new digital design of an equipment for protection relay testing [1]. It is a low cost solution that can be used by the utilities for their laboratory and/or field tests. The simulator enables dynamic tests for protection relays. This is a preferable test approach in the cases when an elaborate evaluation of a relay design is needed [2].

DYNA-TEST Simulator provides test signals from two sources: simulation program and recorded fault data. Simulations are done using the Electromagnetic Transient Program (EMTP), while the fault signals are obtained from Digital Fault Recorders (DFR). These test signals are pre-processed and used by the simulator controller for protection relay testing.

This paper gives results of an evaluation procedure used to illustrate performance characteristics of the DYNA-TEST Simulator. Data pertaining to the source of test signals is taken from Houston Lighting & Power (HL&P) Company, and represents an actual power system fault condition. The simulator hardware performance evaluation data is taken from the simulator design itself and represents specific features of the design.

The first part of the paper is related to the description of the HL&P system modeling approach. The second part gives the comparison of simulated and recorded fault waveforms. The last part of the paper illustrates the performance of the D/A conversion subsystem used for the test signal reconstruction.

HL&P SYSTEM MODEL

The objective of this example is to verify models used in EMTP simulation and demonstrate the accuracy of the test signals obtained using EMTP. In order to do that, the simulated signals will be compared with the actual recordings from a Digital Fault Recorder (DFR) for a single-line to ground fault in HL&P's 345 kV system.

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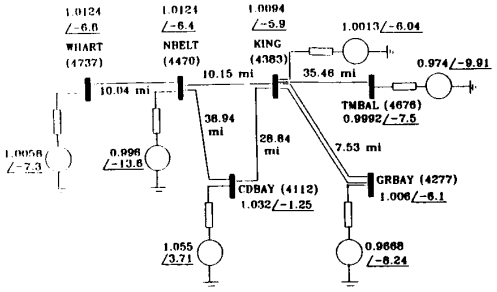

Figure 1. One-line Diagram of the Reduced HL&P System

The 345 kV system is represented by a reduced equivalent system containing 6 buses only. All 345 kV lines that originate from the buses NBELT and KING are represented in detail. The rest of the system is replaced by a 60 Hz short-circuit equivalent. The transmission lines in the study system are modeled either as a FD or CP line, depending on their relative importance, as given in Appendix I. The same Appendix also provides additional modeling data for the lines.

The line section of interest runs from NBELT to KING substation, as shown in Figure 1. A single-phase to ground fault occurred at the NBELT substation. The DFR located at KING recorded all phase voltages and line currents during this fault.

INSTRUMENT TRANSFORMER (IT) MODELS

In order to investigate the IT influence on secondary signal distortion, the CTs, PTs and CVTs located at substation KING have been modeled. The following discussion gives the methodology for model validation. The models adopted are further verified by comparing the recorded and simulated waveforms. This is given in the next section.

CT Model Validation. The CT has been modeled as given in the accompanying paper [1] using the TRANSFORMER model in EMTP. Flux-I characteristic has been calculated from the V-I characteristic using the auxiliary program CONVERT.

In order to validate the EMTP CT model, a CT model based on an analytical approach has been used as a reference [3]. In order to get the same fault current waveform as described by the analytical equation given in [3], the power system model shown in Figure 2 has been used.

Different burdens have been used to investigate the CT behavior. According to the ANSI/IEEE standards, the following burdens have been selected: 8Ω, $j8\Omega$, and B-8 $(4 + j6.93\Omega)$. The simulation results for the analytical and the EMTP CT model (CT ratio 1200/5 A, burden B-8) are given in Figure 3.a and Figure 3.b respectively. As can be observed, the EMTP CT model response is quite close to the analytical model response which demonstrates the validity of the EMTP CT model.

Since the EMTP CT model becomes a part of the complete system model during event simulation, the CT transient response is available simultaneously. This makes the model highly suitable for implementation in the DYNA-TEST Simulator.

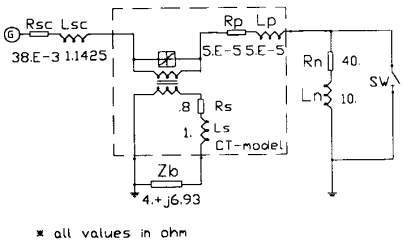

Figure 2. Power System Configuration used for CT Saturation Evaluation

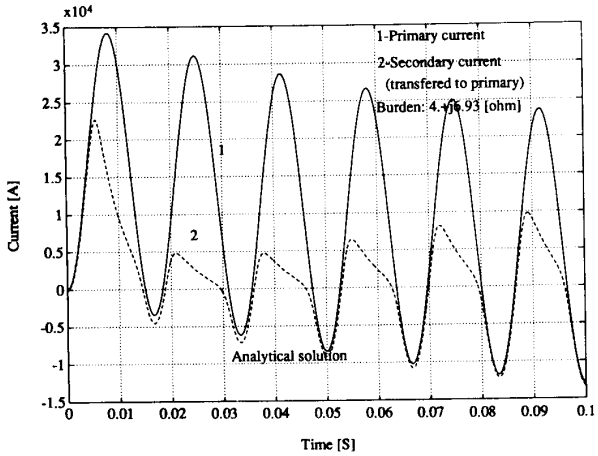

Figure 3.a. CT Transient Response for the Analytical Model (burden B-8)

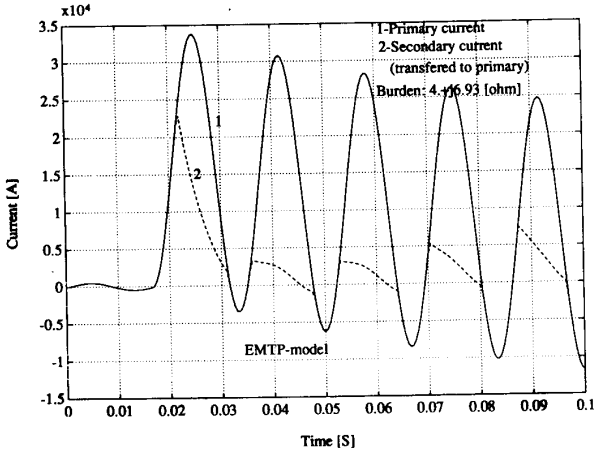

Figure 3.b. CT Transient Response for the EMTP Model (burden B-8)

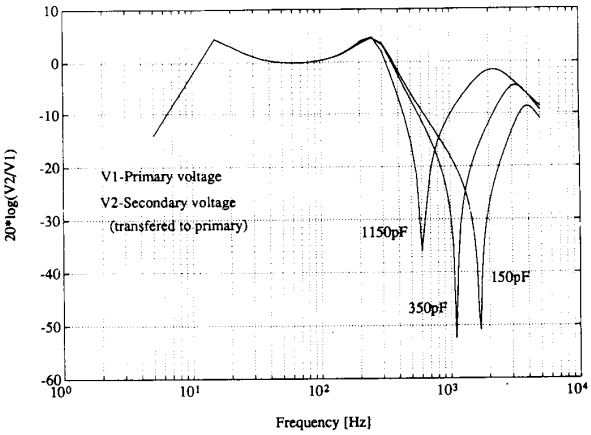

Figure 4. Influence of Compensating Inductor Stray Capacitance on CVT Frequency Response

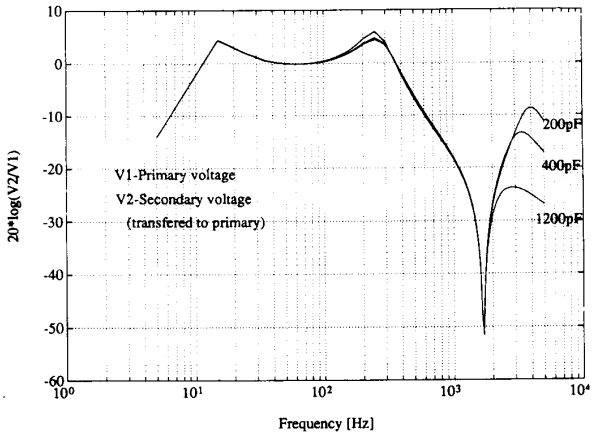

Figure 5. Influence of SDT Primary Winding Stray Capacitance on CVT Frequency Response

PT and CVT Model Validations. The PT has also been modeled using the TRANSFORMER model. The validity of this approach has already been demonstrated in the EMTP documentation.

The CVT has been modeled by including a ferroresonance suppression circuit representing the one used in the actual CVT. The step-down transformer(SDT) has been modeled in the same way as the PT. The CVT data was not requested from the vendor; instead, most of the parameters were measured from an actual CVT that was provided to TAMU by HL&P. Some of the parameters were taken from the CVT documentation. By analyzing the CVT design and using the measured CVT parameters, the CVT model given in the accompanying paper is obtained [1].

In order to investigate the influence of CVT parameters on its frequency response, a parameter sensitivity analysis was performed. The analysis included the following parameters: coupling capacitor, stray capacitances and SDT iron loss resistance. The most interesting results are enumerated below.

The compensating inductor stray capacitance has significant influence in the higher frequency range, as shown in Figure 4. The SDT primary winding stray capacitance also has some influence in the higher frequency range, as shown in Figure 5. The other parameters that were analyzed show an expected behaviour. As a result, the model given in Figure 6 was adopted.

Comparison of the frequency response of the actual CVT with the frequency response of the EMTP CVT model is the

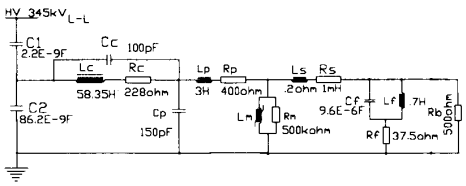

Figure 6. Adopted CVT model

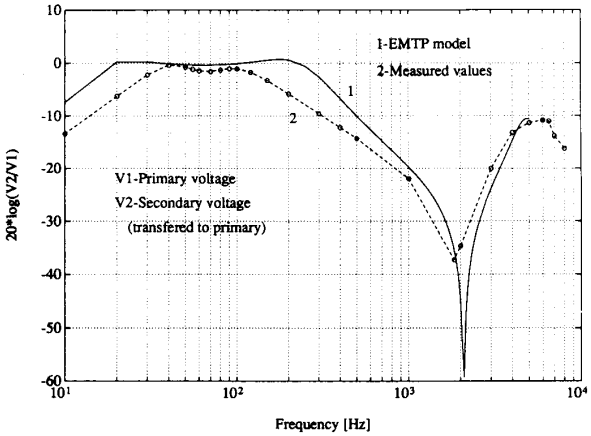

Figure 7. Frequency Response of a Real CVT vs. EMTP CVT model

basis for model validation. Using EMTP, the CVT frequency response has been obtained for both, the actual and the equivalent coupling capacitor(CC) representations in the CVT model. The results obtained show that there is no difference between them; therfore, the equivalent CC model may be used for the CVT transient response analysis.

The frequency response of the equivalent CC circuit of the CVT model was also measured. The tests were done using a 100V sinusoidal signal in the 10 Hz to 5kHz frequency range with a resistive burden of 110 Ω. The results of the measured frequency response of the CVT compared to that obtained from EMTP are shown in Figure 7. It can be noticed that there is a good correlation between the measured and calculated values. The small difference between them exists due to the high-Q ferroresonant suppression circuit, which provides high attenuation at frequencies under and above the fundamental. This is due to the use of a specially designed inductor in the actual CVT. In order to simplify the modeling, the ferroresonance suppression circuit in the EMTP CVT model is represented as shown in Figure 6.

In order to verify that the difference seen in Figure 7 exists only due to the special design of the actual ferroresonant suppression circuit, two test cases have been analyzed. One is a comparison of the frequency response for the actual and adopted ferroresonant supression circuit. The other is a comparison of the frequency response for the actual CVT and the EMTP CVT model, both without the ferroresonant suppression circuit.

Figure 8 shows the difference in the frequency response between the actual and the adopted ferroresonant suppression circuit. Figure 9 shows the small difference between the frequency response of the actual CVT and the EMTP CVT model. The results verify the conclusion given earlier.

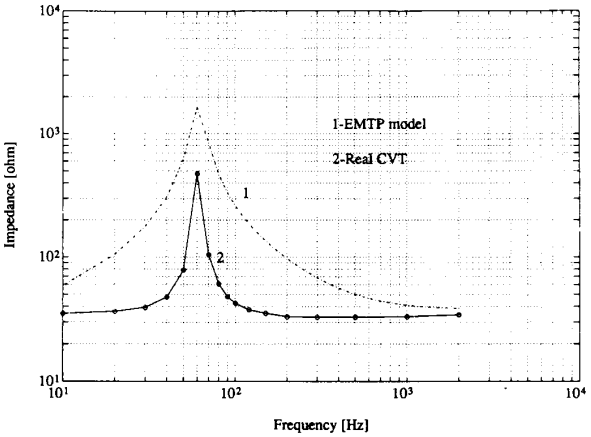

Figure 8. Tuning of Real and Adopted Ferroresonant circuit

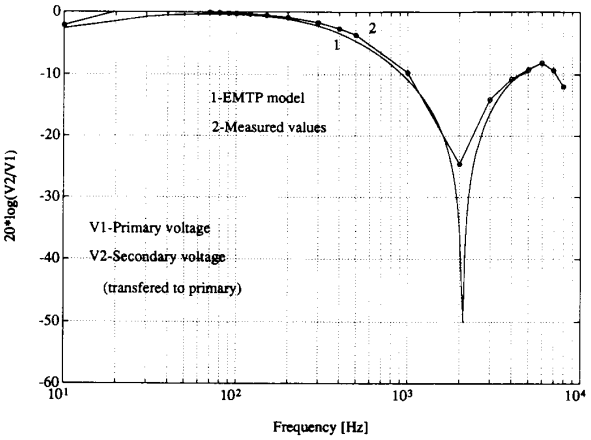

Figure 9. Frequency Response of Real vs. Modeled CVT without Ferroresonance Suppression Circuit

COMPARISON OF RECORDED AND SIMULATED SIGNALS

Recorded signals. The records obtained from the DFR at KING contain three phase voltages recorded at the CVTs and corresponding line currents recorded at the CTs. An additional bus PT is installed in phase A to monitor high frequency transients. Coincidentally, the fault occurred on the same phase, providing valuable information about the actual fault transients.

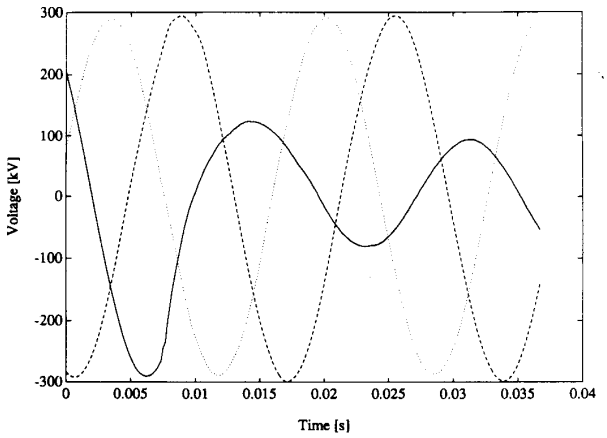

Figure 10.a. Voltage Waveforms Recorded at the CVT Secondaries

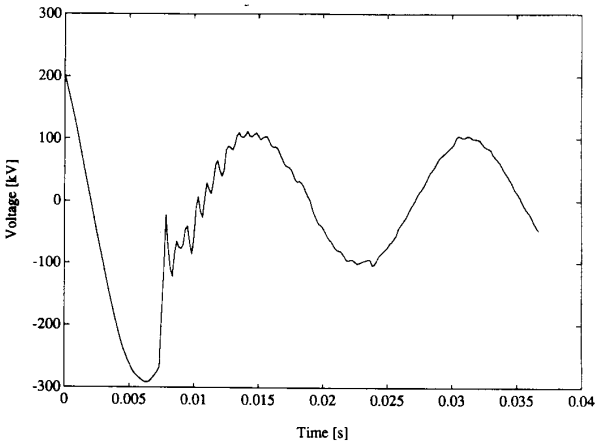

Figure 11.a. Faulted-phase Voltage Waveform Recorded at PT Secondary

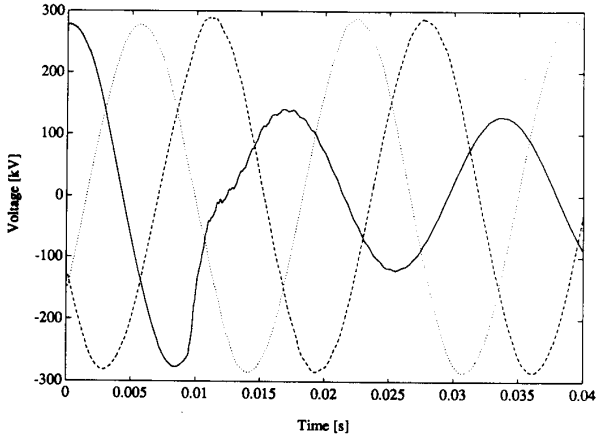

Figure 10.b. Voltage Waveforms Simulated at the CVT Secondaries

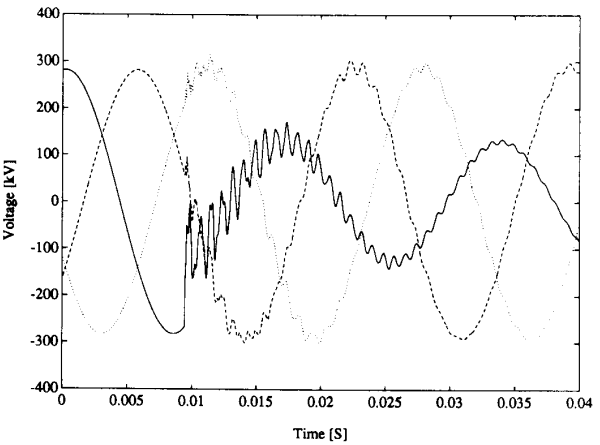

Figure 11.b. Faulted-phase Voltage Waveform Simulated at PT Secondary

The DFR used a sampling rate of 6 kHz to store data. This limits the highest frequency in the recorded signal to less than 3 kHz (Nyquist's criterion). Therefore, the DFR's ability to accurately record high frequency transients was impaired.

Simulated signals. Phase voltages at KING and line currents from KING to NBELT are simulated for a single-line to ground fault located on phase A at NBELT. These signals are computed at the HV system level as well as at the secondaries of the PTs, CTs and CVTs installed at sub station KING.

Comparison. In order to facilitate the comparison of recorded and simulated waveforms, all signals from the IT secondary side have been scaled to the primary side.

Figure 10.a shows the voltages recorded from the CVTs. In order to obtain corresponding simulated waveforms, a complete model of the HL&P study system, including the developed CVT model, was used. The simulation results are given in Figure 10.b. The comparison shows a good agreement between the recorded and simulated waveforms.

In order to validate the accuracy of the system model, the recording of the faulted-phase voltage transient at the bus PT (shown in Figure 11.a) is compared to the voltage transient generated at the PT secondaries by the EMTP simulation. The waveforms generally match, although some difference is observed in their transient part.

In order to further investigate this difference, a frequency analysis of the post-fault part of the waveform is performed for both recorded and simulated signals, as shown in Figures 12.a and 12.b respectively. The analysis shows virtually identical energy contents at all frequencies up to 1 kHz. The main difference is in the 1.2 kHz discrete component amplitude showing $\approx$12 dB mismatch. The higher frequency peaks contained in the simulation output can not be verified against the recording since the frequency is higher than the 3kHz limit of the DFR. However, the component amplitudes in the 1.5 to 3 kHz range (in Figure 12.a) are consistent with the high frequency energy rise that is likely to occur due to aliasing introduced in the recording process.

The recorded and simulated current signals are shown in Figures 13.a and 13.b respectively. The unbalanced phase relationship between the three phases during post-fault conditions can be easily seen from both types of signals. The simulated faulted-phase current does not have as large a D.C. offset as seen in the recorded signal. However, the peak to peak magnitude is nearly the same in both cases. The current spike seen in the recorded signals at the fault instant is actually a feed-through signal generated by capacitive coupling between the voltage and current signals in front of the DFR.

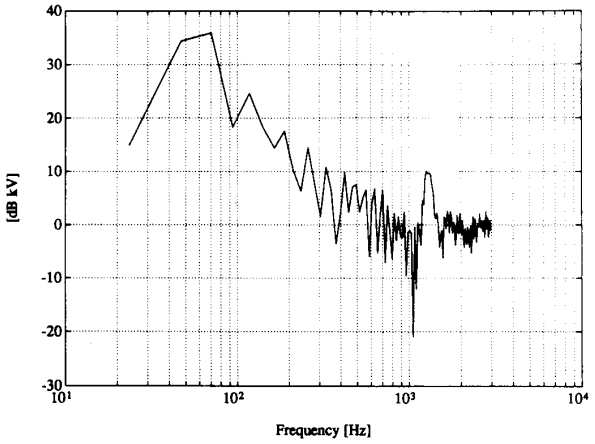

Figure 12.a. Frequency Content of the Post-fault Data taken from Figure 11.a

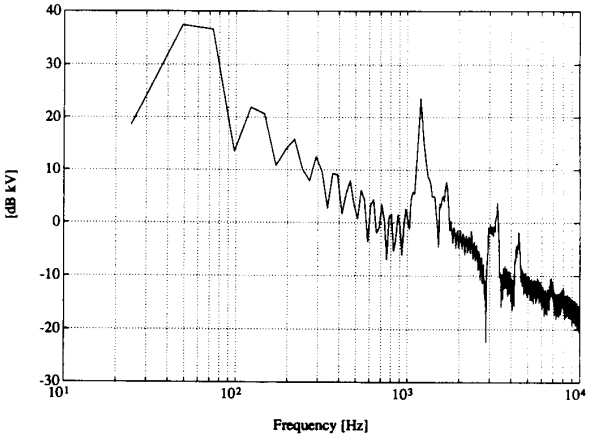

Figure 12.b. Frequency Content of the Post-fault Data taken from Figure 11.b

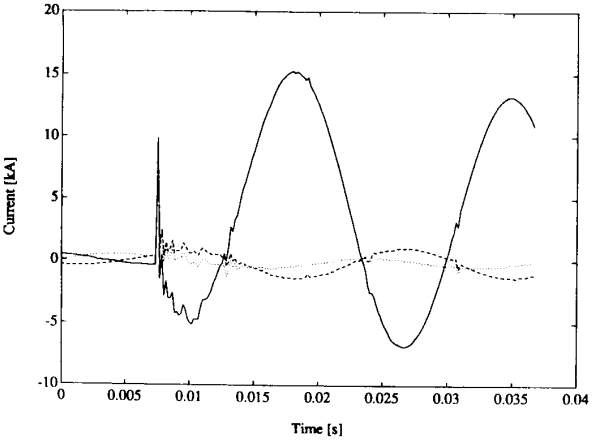

Figure 13.a. Current Waveforms Recorded at the CT Secondaries

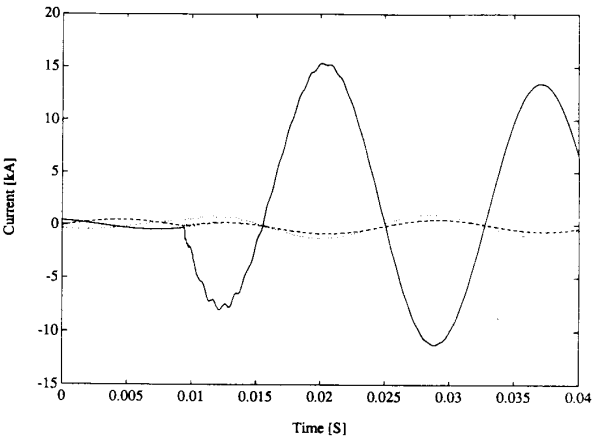

Figure 13.b. Current Waveforms Simulated at the CT Secondaries

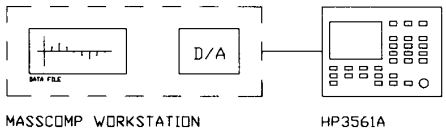

Figure 14. D/A Performance Measurement Setup

HARDWARE PERFORMANCE EVALUATION

D/A Converter Interface

The main question concerning the performance of hardware is: how good is the existing D/A converter interface in terms of the reconstructed waveform precision. The computer is equipped with an 8 channel D/A converter board [4]. In order to measure its performance, a precision sine-wave signal was constructed with the sampled values stored in the data file. The signal was then replayed by the built-in D/A converters, and analyzed with a low frequency FFT-based spectrum analyzer. Measurement setup is shown in Figure 14.

Three sets of parameters were measured: total harmonic distortion level, noise floor, and intermodulation distortion.

Total Harmonic Distortion Level (THD). THD measurements where performed at two different sampling frequencies. Two different data files were used. The first file contained one frequency component with $f = f_s/16$. The second file, intended for intermodulation distortion measurements, contained two frequency components with $f = f_s/3.20855$, and $f = f_s/2.6666$. Signal frequencies were chosen to be non integer multiples of f_s. RMS averaging of 32 data records in frequency domain was done to eliminate the influence of frequency analyzer resolution on measurement precision.

The expected THD can be estimated from the equations valid for the ideal A/D and D/A converters. It is a function of the tested converter resolution [5]:

$$Dynamic\ Range = 6 \cdot N + 1.2 \quad [dB] \tag{1}$$

For an ideal 12 bit D/A converter the dynamic range should be equal to:

$$6 \cdot 12 + 1.2 = 73.2\ dB \tag{2}$$

This is valid only for the harmonically related distortion components. Measured values (THD ≈ -81.5 dB) in Tables

Table II - Harmonic Distortion Level ($f_s = 30kHz$)

FREQUENCY	LEVEL
fo= 1.875 KHz	0 dB
2*fo	-83.49 dB
3*fo	-80.74 dB

THD= -81.49 dB
Noise Floor= -90.49

Table III - Harmonic Distortion Level ($f_s = 16kHz$)

FREQUENCY	LEVEL
fo= 1 kHz	0 dB
2*fo	-84.48 dB
3*fo	-84.92 dB

THD= -81.75 dB
Noise Floor= -90.84 dB

II and III clearly show that the actual D/A converter linearity highly supersedes the minimal requirement (−73.2 dB). This performance is quite acceptable for the simulator.

Other error sources, such as sampling clock jitter or output stage additive noise, add mainly to the system noise floor. In addition, sampling clock jitter also contributes to the harmonic distortion level such that the level of distortion increases proportionally with the increase of input signal frequency and/or amplitude. In most of the practical cases the stability of the sampling clock is sufficient to keep all the unwanted effects below the physical D/A converter resolution.

Noise Floor. In order to check the D/A system behavior, the overall noise floor was measured. The expected values should be lower than the values predicted by equation (1). This is becuse the FFT-based spectrum analyzer used in the measurements performs the averaging of the input waveform. The measured value thus depends on the record length (1024 points) and the choice of the windowing function. According to [5], the signal-to-noise ratio (SNR) of the ideal A/D (D/A) converter measured using the FFT is:

$$snr(ideal) = \frac{10 \cdot \log_{10}(3 \cdot M \cdot 2^{2N})}{ENBW \cdot \pi} \quad [dB] \qquad (3)$$

Where:

M - Total record length

ENBW - Effective Noise Bandwidth for the used window

N - Physical resolution of the conversion system

Since the two-term Hanning window was used in the measurements, ENBW is equal to 1.5 [6]. The expected noise floor is 100.38 dB as calculated according to equation (3). The measured values are slightly higher ($\approx$ 90 dB) due to the resolution limits of the spectrum analyzer , but clearly show the well behaved nature of the measured D/A converter. Measurement results are appended to Tables II and III.

Intermodulation Distortion. The intermodulation distortion test results are shown in Table IV. The test is performed by generating two sinusoidal signals close to the high frequency end of the frequency range and measuring their product component at $f_p = f_2 - f_1$.

As can be seen from the results, the expected spurious component is well suppressed ($\approx$ 63 dB), although still higher than the ideal 73.2 dB limit. This can be attributed to the fact that no deglitcher is used in the circuit and that the actual intermodulation level of the used signal analyzer is not specified.

Table IV - Intermodulation Distortion Level

SAMPLING FREQUENCY	SIGNAL FREQUENCY	LEVEL
f_s= 30 kHz	9.350 kHz	0 dB
	11.250 kHz	-0.2 dB
(I.M. product)	1.900 kHz	-62 dB
f_s= 16 kHz	4.986 kHz	0 dB
	6.000 kHz	-0.6 dB
(I.M. product)	1.014 kHz	-63 dB

Since the probability of occurrence of large-amplitude high frequency components in a typical power system transient signal is fairly small, this distortion is sufficiently low and can be disregarded.

The distortion levels measured show that the tested system possesses sufficient linearity without the use of special deglitching [5] circuitry. This enables complete elimination of this circuitry from the designed reconstruction system.

Overall Accuracy Evaluation

It is obvious that the overall accuracy of the waveform reconstruction system is a function of individual precision of all components in the signal processing chain. The main components of the chain are: D/A converter, timing generator, input buffer, low pass reconstruction filter, output buffer, and power amplifier. Since all of the components involved (except for the power amplifiers) perform low-level analog signal processing, it is realistic to expect a high precision of the output waveform. Furthermore, waveform precision was set up as the main goal in the actual circuit design, requiring that no single component should introduce an error greater than 1 LSB (Least Significant Bit) of the used 12-bit D/A converter. The overall precision is expected to be in the range of 11 Effective Bits (0.05%) at the power amplifier input, regardless of the actual signal level since additional gain switching is built into the design. The overall accuracy at the power amplifier output drops significantly due to the inability of high power devices to provide such a precision. This is especially true in the case of current (transconductance) amplifiers due to the inherent power supply and feedback circuitry design problems. The detailed testing of power amplifiers is therefore of utmost importance in order to predict the actual reconstructed waveform precision for a given application.

CONCLUSION

Evaluation results presented in this paper illustrate the satisfactory performance characteristics of the DYNA-TEST Simulator. The following conclusions can be drawn:

- Methodology used for power system modeling and fault simulation in the HL&P case is valid for any future power system modeling and fault simulation cases.

- Methodology used for IT modeling is quite powerful and enables modeling of any other type of IT that may be required in the future.

- Controller hardware system used in the Simulator design provides accuracy required for the Simulator analog signal reconstruction system.

ACKNOWLEDGEMENTS

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References

[1] M. Kezunović et. al. "DYNA-TEST Simulator for Relay Testing Part I: Design Characteristics",ibid.

[2] CIGRE Report, "Evaluation of Characteristics and Performance of Power System Protection Relays and Protection Systems", CIGRE SC 34, WG 04, Paris, France, 1987.

[3] S. E. Zocholl, W. C. Kotheimer, "An Analytic Approach to the Application of Current Transformers For Protective Relaying" 43. Annual Georgia Tech. Protective Relay Conference, Atlanta, GA.,May 3-5, 1989.

[4] S. Gilbane, "DA 08F Hardware Manual" Order No. 075-04025-00, Massachusetts Computer Corporation, 1985.

[5] "IEEE Trial Use Standard for Digitizing Waveform Recorders" IEEE std. 1057, July, 1989

[6] F. J. Harris, "On The Use of Windows For Harmonic Analysis With the Discrete Fourier Transform" Proceedings of the IEEE, Vol. 66, No. 1, January 1978.

APPENDIX I.

The transmission lines in the study system are modeled as listed in Table I.1. The line parameters for the CP line models are given in Table I.2. The data for the FD line models and the tower geometry are given in Table I.3 and Figure I.1 respectively.

Table I.1. Transmission Line Models Used

Transmission Line	Type of Line Model
KING - NBELT	FD Line
KING - TMBAL	CP Line
KING - CDBAY	FD Line
KING - GRBAY	CP Line
NBELT - CDBAY	FD Line
NBELT - WHART	CP Line

Table I.2. CP Line Model Parameters

Line Designation	Length (miles)	R'_0 Ω / mi	$\omega L'_0$ Ω / mi	$\frac{1}{2}\omega C'_0$ μ mho/mi	R'_+ Ω / mi	$\omega L'_+$ Ω / mi	$\frac{1}{2}\omega C'_+$ μ mho/mi
KING - TMBAL	35.46	0.33	1.719	4.047	0.0346	0.5636	7.271
KING - GRBAY	7.53	0.36	1.617	4.541	0.0537	0.5738	6.895
NBELT - WHART	10.04	0.38	1.733	4.325	0.0557	0.5690	6.423

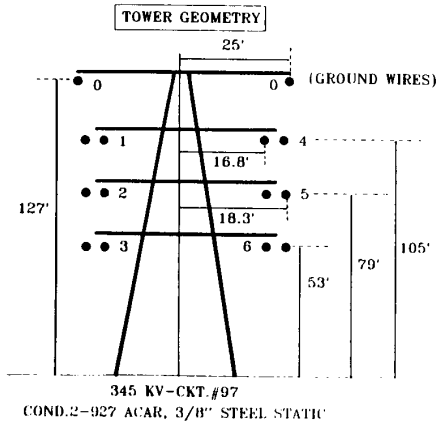

Figure I.1. Tower Geometry

Table I.3. Data for FD Line Models

Conductor Type	Max. Outside Diameter (inches)	A.C. Resistance (Ω/mi)
Ground 3/8" Steel Static	0.36	7.565
Phase 927 ACAR ALCOA	1.108	0.1193
Earth Resistivity = 30 Ω meter.		

Mladen Kezunović (S'77, M'80, SM'85) received his Dipl. Ing. degree from University of Sarajevo, Yugoslavia, the M.S. and Ph.D. degrees from University of Kansas, all in electrical engineering in 1974, 1977, and 1980, respectively.

Dr. Kezunović's industrial experience is with Westinghouse Electric Corporation in the U.S.A., and the Energoinvest Company in Yugoslavia. He also worked at University of Sarajevo, Yugoslavia. He was a Visiting Associate Professor at Washington State University and at Texas A&M University, for the 1986-1987 and 1987-1989 academic years, respectively.

Ali Abur (M'86, SM'90) received the B.S. degree from METU, Turkey in 1979, the M.S. and Ph.D. degrees from The Ohio State University, Columbus, Ohio, in 1981 and 1985 respectively.

Since late 1985, he has been an Assistant Professor at Texas A&M University, College Station, Texas.

Ljubomir Kojović received his Dipl. Ing. degree from University of Sarajevo, Yugoslavia, the M.S. degree from University of Belgrade, and Ph.D. degree from University of Sarajevo, all in electrical engineering in 1972, 1977, and 1981, respectively.

From 1972 up to now he is with Energoinvest Company, Sarajevo, Yugoslavia. He is also an Assistant Professor at the University of Tuzla, Yugoslavia. During the Summers 1989, 1990 he was with Texas A&M University as a post doctorate research associate.

Veselin Skendžić (M' 88, S' 90) received his Dipl. Ing. degree from University of Split, and M.S. degree from University of Zagreb, Yugoslavia, all in electrical engineering, in 1983 and 1990, respectively.

From 1984 to 1989 he was with Electrical Engineering Department at the University of Split. Currently he is a graduate student at Texas A&M University.

Harinderpal Singh (M' 86, S' 88) received his B.S (Honors) degree from Panjab University, India, in 1983 and M. Tech. degree from Indian Institute of Technology, Bombay, in 1985, both in Electrical Engineering. Currently he is doing research toward a Ph.D degree at Texas A&M University.

From 1985 to 1987 he worked as an Application Engineer in the Switchgear division of Voltas Ltd., Bombay.

Charles W. Fromen (M' 68, SM' 85) was born in Atlanta, Georgia, on March 11, 1944. He received a Bachelor of Science Degree in Electrical Engineering from Texas A&M University in 1968. Upon graduation, Mr. Fromen joined Houston Lighting & Power Company. He was assigned first to the Distribution Relay Protection Group in 1968. Then he was assigned to the Transmission & Generator Relay Protection Group in 1971. Since 1984 he has had the title of Consulting Engineer. He is the HL&P Co. technical representative for the East Tie HVDC Project.

Mr. Fromen has been the HL&P Co. representative to the IEEE Power Systems Relaying Committee since 1973 and is a member of the Relay Practice Subcommittee. He is a Registered Professional Engineer in the State of Texas.

Donald (Don) R. Sevcik (M' 81) was born in El Campo, Texas in 1953. He received his Bachelor of Science Degree in Electrical Engineering from Texas A&M University in 1975.

Mr. Sevcik is employed by Houston Lighting & Power Company in 1975 and is presently a Lead Engineer. Has worked in the following areas: Power Plant Electrical Systems (1975 to 1977), System Studies (1977 to 1979), and Transmission and Generation Protection (1979 to present).

Mr. Sevcik is a Registered Professional Engineer in Texas. He is a former officer of the Houston Chapter of the Power Engineering Society.