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### INTRODUCTION

Application of microprocessor to protective relaying of Electric Power Substations started in the mid 70-ties. A number of microprocessor based protective relays were developed up until today and some of those were extensively tested in the Power Substation environments. Some of the microprocessor based relays are commercially available, but most of them are still in the development stage. Typical example of the latest developments are Microprocessor Based Distance Relays which are not commercially available yet.

One of the most critical subsystems of a microprocessor based relay is the Data Acquisition Unit (DAU). It transforms analog input signals into a digital form suitable for further numerical processing associated with numerical protective relaying algorithm. Performance of the overall relay is very much dependent on DAU, and this subsystem should be carefully designed in order to satisfy quite severe data acquisition requirements.

This paper describes design requirements, implementation characteristic and performance analysis related to a Microprocessor Based DAU which was developed for digital protective relaying applications. First section of the paper defines design requirements. Second section gives a brief survey of the possible approaches that could be taken in designing such a unit. Third section is related to characteristics of the Microprocessor - based DAU which was implemented. Finally, some performance analysis results are given at the end.

### DESIGN REQUIREMENTS

All of the requirements can be classified into two categories: system and application requirements. DAU discussed in this paper is used for the Distance Relaying application. Therefore, there is a close relation between system requirements

of a Distance Relay and the DAU system requirements. This relation is represented in Table 1.

Application requirements include: input signal and protective relaying algorithm matching, time and frequency response, data acquisition sampling rate.

Input signal matching requirement includes need for appropriate isolation levels on input terminals of DAU. Those levels should be matched to the specific situation regarding voltage and current signals in the substation environments. Mentioned requirements are specified with a number of standards defined by the IEC and national standards organisations such as BEAMA in U.K., ANSI/IEEE in USA, VDE in West Germany. Input signal requirements also ask for linearity of input signal in the range  $0-20I_n$  and  $0-2U_n$  for the current and voltage signals respectively.

Protective relaying algorithm matching requirement is related to the output of DAU which is delivered to the measurement unit in the Distance Relay. This output signal should be in a form suitable for further digital algorithm processing. This requirement translates into requirement for two's complement form of the output signal as well as into requirement for signal coefficients adjustment needed for the protective relaying algorithm calculations (1).

Time response is related to the fault clearance time which is in the order of one power cycle time. Frequency response depends on the frequency characteristics of the input signal as well as on the sampling rate implemented. Therefore the frequency response requirement translates into antialiasing filter design requirement.

TABLE 1 - Distance Relaying System Requirements

<u>Design Criterion</u>	<u>Distance Relaying Requirements</u>	<u>DAU Requirements</u>
1. Utilization	Processor execution time and memory utilization	Adjustable for various protective relaying applications
2. Flexibility	Application flexibility to accommodate various protection requirements	Software modularity
3. Simplicity	Simple to operate and visible indications	Simple to interface to the switchyard and to the relay and to configure for various applications
4. Accuracy	≤ 5%	Selection of the appropriate A/D converter range and data acquisition sampling rate
5. Safety	Fail-safe features	Blocking of operation on Autoranging and Autocalibration test failures
6. Reliability	Continuous self-checking	Continuous self checking
7. Maintainability	Various diagnostic features	Easy to replace and facilities for trouble shooting
8. Cost/Performance	Commercial Market competitive design	Architecture and component selection

SURVEY OF THE DESIGN APPROACHES

This section gives a survey of the possible approaches which can be taken in designing DAU. Topics discussed are: level of processing intelligence, Organization of the data conversion circuitry, Type of antialiasing filters, input signal sampling rate, A/D converter bit resolution, Type of error detection and diagnostic test.

Level of processing intelligence is related to the use of a CPU. Some solutions contain a CPU on DAU (2). In this case DAU is quite independent from other parts of the relay regarding execution of the data acquisition functions. However, there are approaches which do not utilize a CPU unit and in this case data acquisition functions are performed by a specialized circuitry which is dependent on the CPU located elsewhere in the relay.

Organization of the data conversion circuitry can be used either on serial or on parallel conversion. Serial conversion is implemented using a single A/D converter per several channels, which needs a multiplexer to select one channel at the time (1).

Parallel conversion assumes that there is an A/D converter per channel (3). serial conver-

sion is cheaper, but it is slower than the parallel conversion.

Type of antialiasing filters depends on the characteristics of input signals and the sampling function. Most often used are two-pole (4) and three-pole(3) low pass or band pass filters. Implementation of the filters is either analog (3) or digital (5).

Input signal sampling rate is selected based on the algorithm characteristics. It is usually selected between 4 to 24 samples per power cycle (4, 6).

Bit resolution of the A/D converter is selected to be between 10 and 16 bits (6, 1). There are number of tests implemented in DAU. Those tests usually include: autocalibration, autoranging, self-test of power supply, watch dog timer, memory and processor self-tests (1, 3).

CHARACTERISTICS OF THE DAU

This section gives description of the Microprocessor - Based DAU which was implemented. Also a brief discussion of the criteria for component selection is outlined.

A block diagram of DAU is given in Figure 1. As it can be seen, input signal is first brought to the isolation and scaling circuitry. After

that, the signal goes to an electronic switch whose position is selected by the software. Positions are either "test" or "normal". In the "test" position it is possible to correct offset and gain. It is performed by applying a known referent voltage and by measuring the error in the circuit output. Referent voltage for the offset correction is 8 V, and referent voltage for the gain correction is some known voltage level i.e.  $\pm 5V$ . Each channel is corrected using this scheme.

Choice of the S/H circuit is dependent on the stabilizing time of the output signal and on the price. Since each channel is equipped with an S/H circuit, it is not needed that stabilizing time be shorter than 5  $\mu$  sec.

Selection of the A/D converter includes consideration of the several factors. If one selects a fast A/D converter with the conversion time of several microseconds, it would be possible to perform two conversions per each sample of a signal. This will enable optimal gain adjustment. However, this solution is not acceptable because of the high cost of those converters. Hence, selected are A/D converters with the conversion time in the range of 20-30 microseconds.

A/D bit resolution should be selected taking into account expected levels of the input signal. Therefore, it is decided to select a 12 bit A/D converter and use a programmable gain

circuitry to provide 16 bit resolution for small signals. Programmable gains selected are  $\times 1$  and  $\times 8$ . Converted value is shifted (multiplied) if it is needed and prepared in the two's complement format for further processing.

Selection of the CPU used to control Digital circuitry and to process converted data depends on the required processing load. An 8-bit CPU is acceptable in this case.

Software should be organized in such a way so that overall A/D conversion is performed in the shortest possible time. Because of that, it is needed to utilize the CPU processing resources in the best way. While A/D conversion of one channel is performed, processor is used to switch related circuitry to the next channel and appropriate offset and gain corrections are performed. When a conversion is completed then, while the processing of the converted data is performed, the next channel is stored for A/D conversion by S/H2 circuit.

Test programs are performed upon completion of conversions for all channels. Only one channel is tested and only one test is performed at the time during the available time between each sample. The choices of tests are: offset correction, gain correction, allowed output signal range check. The timing unit is used to sequence program execution so that indications of error detection and program execution failure are immediately given.

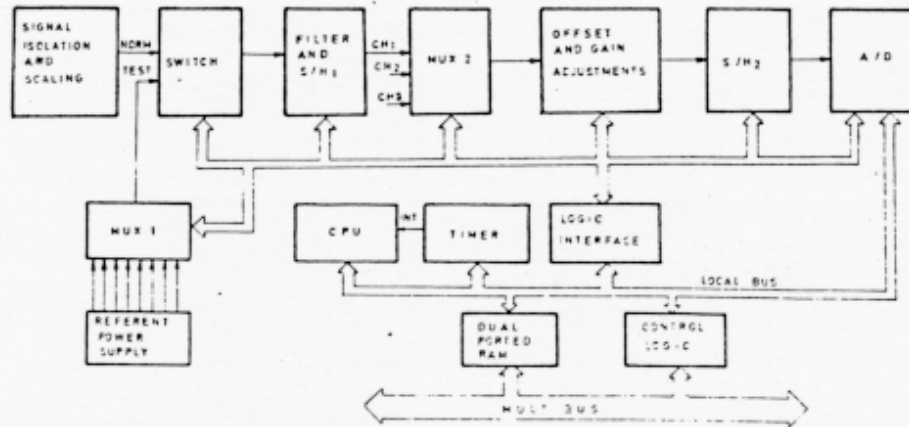


Figure 1. Block diagram of the DAU

## PERFORMANCE ANALYSIS

Performance analysis performed so far includes: static input signal test, dynamic input signal test, nonlinearity estimates, analytical error analysis.

Static input signal test is performed by providing a constant signal level at the DAU input. Results of the conversion are then compared with the known input values. For an ideal case current signal conversion error in the last bit is given by the Figure 2.

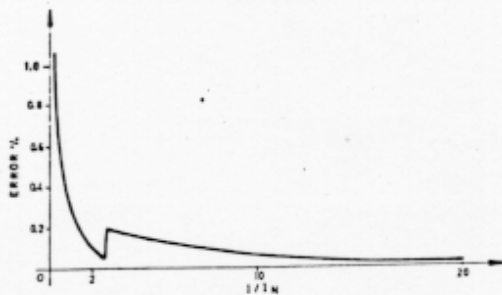


Figure 2. Conversion error diagram

It can be observed that the gain switching point is 2.5 In. It should be noted that some shielding techniques should be applied to improve noise protection and to reduce measurement errors.

Dynamic test is performed by using the referent power supply. Various signal levels are selected by an appropriate resistor network. Those signals are connected to the separate channels. Test procedure is performed by switching various channels and measuring response time of the circuitry. Typical measurements diagrams at the output of MUX 2 and the input of S/H2 are given in Figure 3.

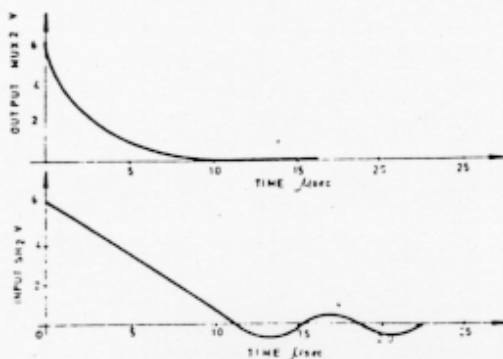


Figure 3. Dynamic signal response diagrams

Nonlinearity analysis shows that special attention should be paid to the DAC and A/D circuits. Typical nonlinearity error for an 8-bit DAC is 0.2%, and for A/D converter  $\pm 1/2$  LSB.

Analytical error analysis is performed based on the data provided in the component catalogs. It can be calculated that voltage drift caused by the leakage currents is 0.1 mV. Offset error of the S/H circuit for the given temperature range (0-70°C) is  $\pm 20$  mV. Similar analytical error analysis can be performed for the multiplexer as well. Offset error is 0.4 mV and time constant is 24 nanoseconds. Operational amplifiers used introduce offset error less than 3 mV.

Overall analysis shows that offset error correction requirements are in the range of 50 mV.

## CONCLUSIONS

The Microprocessor - based DAU presented in this paper represents a very flexible and yet not very expensive solution. It is important to note that use of microprocessors enables implementation of a quite sophisticated measurement correction and operational testing schemes. It is also interesting to note that the DAU performs several preprocessing operations related to the Distance Relaying Algorithm. In this way the main processor processing load is reduced which enables more efficient implementation of the overall relay.

## REFERENCE

- (1) J.P. Jauch "An A to D Converter For Power System Relaying", A.I.M. Conference, Belgium, June, 1981.
- (2) K. Srinivasan, R. Jutras "Programmable Front End For Power Network Parameter Monitoring" IECI 83, U.S.A.
- (3) P. Bornard, J.C. Bastide "A Prototype of Multiprocessor Based Distance Relay" IEEE TPAS Vol. 101, No. 2 February 1982.
- (4) E.O. Schweitzer, et.al. "A Prototype Microprocessor - based System For Transmission Line Protection and Monitoring" Western Protective Relay Conf. U.S.A. October, 1981.
- (5) S. Jayasurya, W.J. Smolinski "Design and Test Log of a Microprocessor - based Distance Relay" IEEE/PES Summer Meeting, Paper No. 83 SM 412-4, U.S.A. July 1983.
- (6) J.V.H. Sanderson, et.al. "Microprocessor Based Distance Relaying - Some Design Considerations" IEE Conf. on Development in Protective Relaying, England, 1980.