

Locating Sub-Cycle Faults in Distribution Network Applying Half-Cycle DFT Method

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Abstract—It is necessary to accurately detect and locate sub-cycle faults in order to prevent unexpected outages. However, conventional fault location methods cannot locate these faults as typically data windows longer than the fault’s signature are used for phasor extraction. This paper presents an overall analysis of how the single-phase-ground sub-cycle fault in the distribution network can be located using voltage sag. The half-cycle Discrete Fourier transform is used for phasor extraction in the time-domain simulations. Our results reveal that the proposed approach is capable of accurately locating sub-cycle faults whose duration is between 0.5 and 1.0 cycles. The results also suggest that the placement of meters may significantly affect the capability of the proposed approach to locate sub-cycle faults.

Index Terms—Fault location, power distribution faults, power system faults, power system protection, smart grids.

I. INTRODUCTION

Fault location has become an essential tool for reliability and outage management of utility services. Various research efforts have focused on fault location methods in distribution systems [1]-[20]. These techniques have culminated in an ability to provide rather accurate solutions [18]–[20]. Most current fault location algorithms require phasor information to be extracted from voltage and current steady-state sinusoidal signals during the fault period.

However, there are also faults whose signal signature is shorter than one cycle, known as sub-cycle faults; some real examples can be found in [21]-[23]. In this case, it is critical that intermittent faults are correctly located in order to prevent unexpected outages. Yet, conventional fault location methods cannot locate these faults because the phasor information during fault period cannot be captured using full-cycle Discrete Fourier transform (DFT) method. Other external disturbances that could affect the accurate calculation of phasors include frequency deviation, random noise, and error in detection of zero-crossing and the fault inception instant.

There have been phasor estimation methods based on samples from short time windows proposed to solve the problem, among which are the improved DFT method [24], recursive wavelet [25], and adaptive signal processing [26], [27]. After reviewing the literature it appears that there are no

systematic fault location methods that could handle sub-cycle faults in distribution networks.

In this paper we quantify the performance of a sub-cycle fault location method which uses voltage sag data extracted with the half-cycle DFT method. As stated in the IEEE Standard C37.114TM Section 6.10 [4], due to the requirement of signal extraction, the traveling wave method may provide the only solutions for short duration faults. In this paper, we attempt to demonstrate that the voltage sag based method may provide solutions as well. We have found that the sub-cycle fault can be located accurately with our method when no additional disturbances are present. Our results also show that the placement of meters may greatly influence the ability of the proposed algorithm to locate sub-cycle faults.

II. BACKGROUND

A. Half-cycle DFT method

Our main interest is the phasor estimation using the half-cycle DFT method. Implementation details for full-cycle DFT can be found in [28]. In the first step of this procedure, we obtain the full-cycle DFT phasor estimation. Let us consider a sinusoidal signal $z(t)$ with fundamental frequency f_0 , phase ϕ , and magnitude Z . Let us assume

$$z(t) = \sqrt{2}Z \sin(2\pi f_0 t + \phi). \quad (1)$$

Now let us assume $z(t)$ is sampled N times in every cycle so that the set of samples $\{z_k\}$ can be obtained as

$$z_k = \sqrt{2}Z \sin\left(\frac{2\pi}{N}k + \phi\right). \quad (2)$$

Then we may use an integer m in the transfer domain which corresponds to the frequency mf_0 in order to extract a particular frequency. To extract the fundamental frequency component m is 1. Thus, the DFT of z_k having the fundamental frequency component can be written as

$$Z_1 = \frac{2}{N} \sum_{k=0}^{N-1} z_k \exp(-j \frac{2\pi}{N}k). \quad (3)$$

We apply Euler’s formula for Z_1 to obtain

$$Z_1 = Z_{\cos} - jZ_{\sin}, \quad (4)$$

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where $Z_{\cos} = \frac{2}{N} \sum_{k=0}^{N-1} z_k \cos(\frac{2\pi}{N}k)$ and

$$Z_{\sin} = \frac{2}{N} \sum_{k=0}^{N-1} z_k \sin(\frac{2\pi}{N}k).$$

Since we are working with a sliding window of the signal, where each window has the most recent N samples, we let Z_{\cos}^{window} and Z_{\sin}^{window} represent Z_{\cos} and Z_{\sin} components at the w^{th} window, respectively. Then we obtain

$$Z_{\cos}^{window} = \frac{2}{N} \sum_{k=w}^{N+w-1} z_k \cos(\frac{2\pi}{N}k), \quad (5)$$

and

$$Z_{\sin}^{window} = \frac{2}{N} \sum_{k=w}^{N+w-1} z_k \sin(\frac{2\pi}{N}k). \quad (6)$$

Our main interest is the fundamental phasor component in the signal obtained from half-cycle DFT. Restricting a sliding window from one cycle to half cycle does not affect the final results of (5) and (6), provided that we have half of N samples per half cycle. In this case, we can rewrite z_k as

$$z_k = \sqrt{2}Z \sin(\frac{\pi}{N}k + \phi). \quad (7)$$

Therefore, by repeating the steps we can obtain the phasor estimation from half-cycle DFT that

$$Z_{\cos}^{window} = \frac{2}{N} \sum_{k=w}^{N+w-1} z_k \cos(\frac{\pi}{N}k), \quad (8)$$

and

$$Z_{\sin}^{window} = \frac{2}{N} \sum_{k=w}^{N+w-1} z_k \sin(\frac{\pi}{N}k). \quad (9)$$

B. Distribution Network Under Study

To test the accuracy and performance of the proposed sub-cycle fault location algorithm we used a model 25 kV distribution network known as the Saskpower network, shown in Fig. 1. Details of network components can be found in [1] and [20].

III. VOLTAGE SAG UTILIZATION FOR SUB-CYCLE FAULT LOCATION ALGORITHM

A. Identifying fault starting time and faulty phase

The method of calculating the duration of a sub-cycle-fault has been discussed in [22]. In this paper we assume that the fault is a single-phase-ground sub-cycle fault. We modify the method described in [22] in order to identify the fault starting time and the faulty phase as shown in Fig. 2.

B. Sub-cycle fault location algorithm

As demonstrated in [16] and [17], matching voltage sag data during the fault period can accurately locate the fault. Since the voltage sag data of a sub-cycle fault can be obtained by applying the half-cycle DFT method, we follow the methodology described in [16] and [17]. First the voltage sag data recorded at measurement nodes is delivered to the distribution local control center. Then, the detected voltage

sag ($V_{recorded}$) can be compared to the calculated voltage sag ($V_{calculated}$) obtained from time-domain simulations. To obtain the characteristic voltage $V_{calculated}$ at the control center, the fault is simulated at each node, one at the time, in the network. The node which has the best match between the actual data $V_{recorded}$ and the calculated data $V_{calculated}$ is the node where fault is detected.

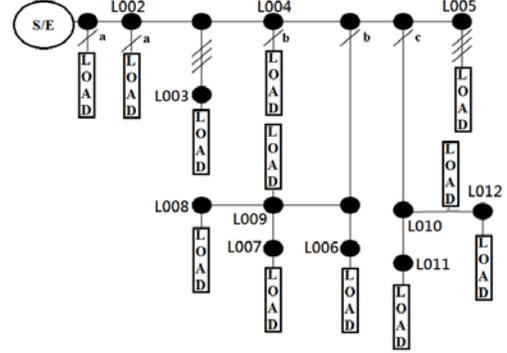


Figure 1. Saskpower network, Canada [1] [20].

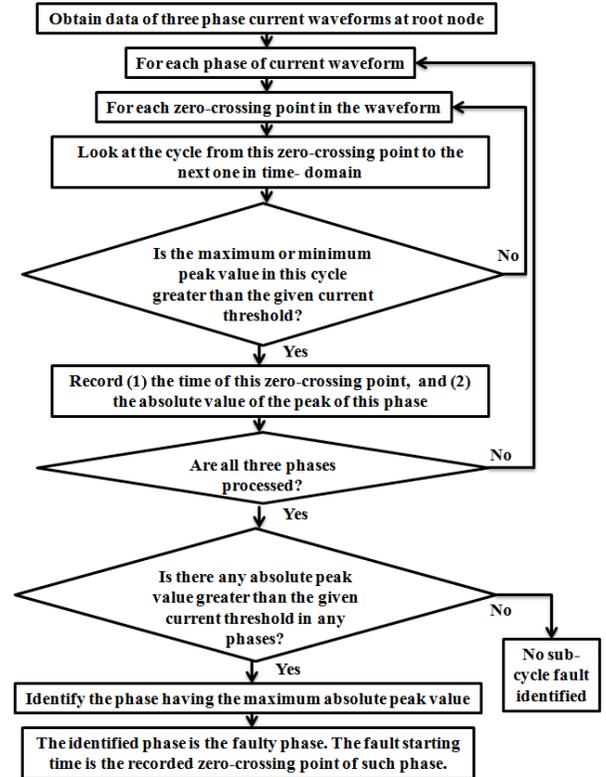


Figure 2. The procedure of identifying fault starting time and faulty phase.

Sometimes when the fault resistance is small, the meters along the feeder may have similar $V_{recorded}$ which increases the difficulty of identifying the fault. In this case the current phase information at the root node can help. More details can be found in [16] and [17].

To summarize the utilization, we apply the findings in [17] so that

$$Error = \varepsilon_{amplitude}^2(V) + \varepsilon_{phase}^2(V) + \varepsilon_{phase}^2(I), \quad (10)$$

and

$$Flag = \frac{1}{Error + \Delta}, \quad (11)$$

where $\varepsilon_{amplitude(V)}$ is the difference between the amplitude of $V_{recorded}$ and $V_{calculated}$, $\varepsilon_{phase(V)}$ is the difference between the phase of $V_{recorded}$ and $V_{calculated}$, $\varepsilon_{phase(I)}$ is the difference between the phase of calculated and recorded current at the root node, Δ is a small number to prevent the division by zero, and $Flag$ is used to identify the fault node.

After the comparison, whichever node has the largest flag value (11), or the smallest error in (10), is the fault node. The details are shown in Fig. 3.

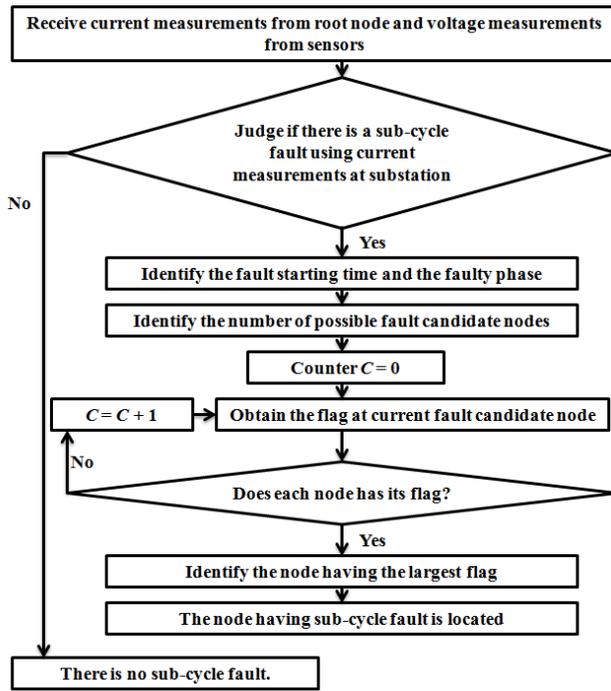


Figure 3. The process of proposed sub-cycle fault location.

The possible candidate fault nodes are obtained by eliminating nodes which cannot be the fault node, so that algorithm efficiency is increased. For instance, if the faulty phase is at phase C, as identified using the current at the root node [22], then those nodes which do not have phase C cannot be the faulty node and therefore are not candidate fault nodes.

In this paper, the following details are not taken into account, and are left for future work:

- Optimization of the meter placement ;
- Sensitivity analysis to external disturbances;
- The full characteristic of current-limiting fuses (CLF) [29].

The optimal meter placement has been fully analyzed in [18] using the network from Fig. 1 as an example. The goal for the optimal placement is to minimize the cost but still provide the accurate results, which is illustrated in [18].

While the characteristic of CLF during the fault period is not fully considered, it appears, based on the previous work

[14]-[18] that the fault location could be identified based on the voltage sag information. The proposed method could be used for the sub-cycle faults as we assume the maximum voltage sag is recorded during the CLF operation.

IV. RESULTS AND ANALYSIS

We have run the cases using Alternative Transient Program (ATP) [30] to obtain the phasor information of the sub-cycle fault from time-domain simulations. Equations (8) and (9) have been implemented in MODELS [30] which is a general-purpose description language used to extract the phasor information. The sampling frequency is set to be 32 samples per cycle.

A. Results of half-cycle DFT method

To demonstrate that the half-cycle DFT method can be used to obtain phasor information correctly during sub-cycle faults, we compare signals extracted using full-cycle DFT with half-cycle DFT in Fig. 4. The signal in blue is the original voltage waveform, red is the rms value from half-cycle DFT, and green is the rms value from full-cycle DFT. The voltage waveform is obtained at the single-phase-ground location. Fault resistance is set to be very close to zero so that voltage drops to zero during the fault period. This illustrates how the data changes during the fault period. As expected the voltage rms data extracted from half-cycle DFT goes to zero, unlike data extracted using full-cycle DFT. We may conclude that voltage sag data can be successfully obtained by applying half-cycle DFT in cases where full-cycle DFT may not be appropriate.

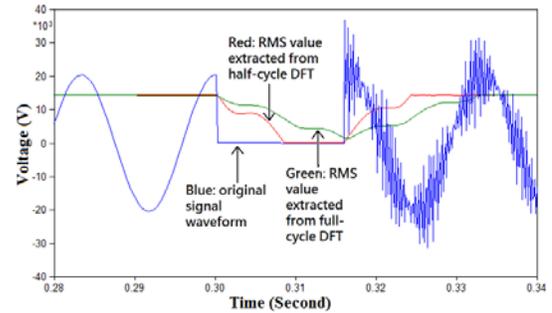


Figure 4. Comparison between data extracted from full-cycle and half-cycle DFT.

B. Validation of the algorithm

To validate if the single-phase-ground sub-cycle fault can be located successfully, we placed the fault at all phases of all nodes indicated in Fig. 1. Since this is to show the correctness of the algorithm and we are not discussing the optimization of the meter placements in this paper, the meters are placed at all the nodes.

The results show that all the faults are successfully located while they are put at difference phases of different nodes. The following cases are shown as examples.

- Case 1. Fault at Node L002 Phase A.
- Case 2. Fault at Node L003 Phase B.
- Case 3. Fault at Node L007 Phase B.
- Case 4. Fault at Node L012 Phase C.

The results show that all the faults are successfully located while they are put at difference phases of different nodes, which we show Cases 1 to 4 as examples. Figs. 5(a), 5(b),

5(c), and 5(d) demonstrate the results of Case 1, 2, 3, and 4, respectively. One can see that the flag value at the fault location is much greater than others at other locations, which applies to all other validation cases.

C. Effect of different meter placements

Although optimal placement of meters is not considered here, our results shown in this section reveal that meter placement may adversely affect the accuracy of the proposed algorithm. In this case, five meters are placed at L002, L003, L004, L009, and L010. Only half of the network nodes have meters, unlike Section IV-B where the meters are placed at all nodes. Illustrating the same four cases described in Section IV-B, Figs. 6(a), 6(b), 6(c), and 6(d) demonstrate the results of Case 1 (fault at Node 002A), Case 2 (fault at Node 003B), Case 3 (fault at Node 007B), and Case 4 (fault at Node 012C), respectively, where we see the fault is located correctly in Cases 1 and 3 but not in Cases 2 and 4.

In Case 1, the flag value at the fault location is much greater than at other locations. In Case 2, the flag values are almost identical at L006, L003, and L009, and similar results are evident in Case 3. This implies that the algorithm cannot differentiate the fault location exactly in Cases 2 and 3. In Case 4, the algorithm wrongly identifies the fault location at another end of the feeder. Comparing Figs. 5 and 6, one can see that only the results of Case 1 show a similar pattern where other cases do not. Therefore, the placement of meters may significantly affect how effective the algorithm is.

V. CONCLUSIONS

This paper makes several contributions:

- A sub-cycle fault location algorithm is implemented using voltage sag data obtained from time-domain simulations and half-cycle DFT.
- The experimental results from using the proposed algorithm suggest that the single-phase-ground sub-cycle fault between 0.5 and 1.0 cycle can be located when no other external disturbances are presented.
- The placement of meters may affect the capability of the proposed algorithm to locate sub-cycle faults: in some cases when we only placed half of the meters in the network the fault cannot be accurately located.

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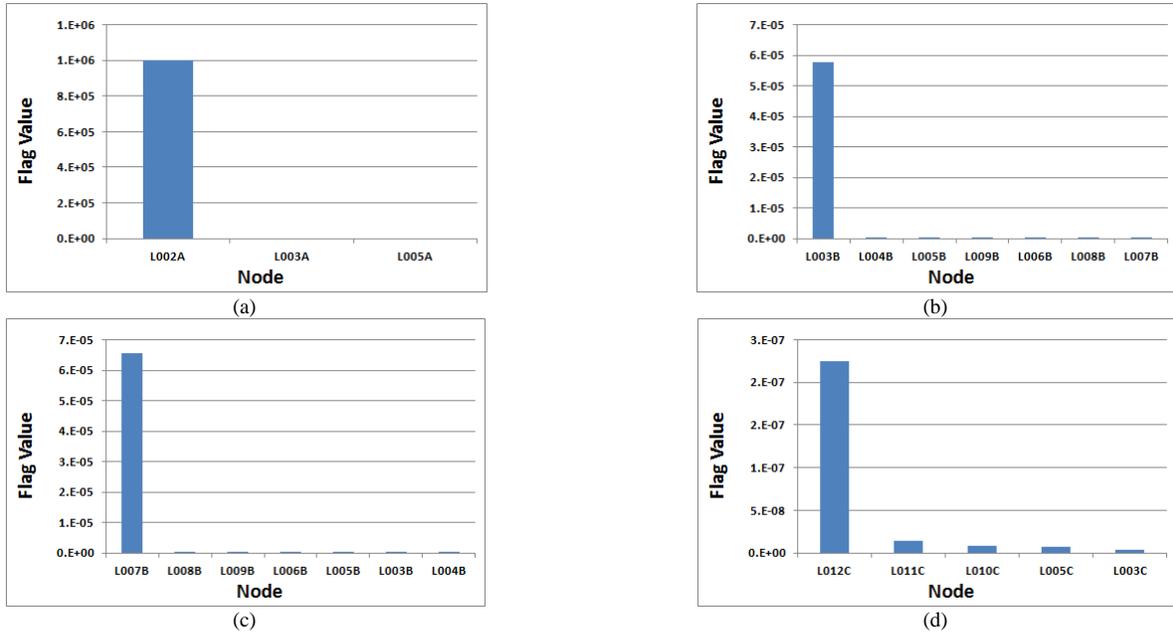


Figure 5. Results of cases, meters at all nodes: (a) Case 1 fault at L002A; (b) Case 2 fault at L003B; (c) Case 3 fault at L007B; (d) Case 4 fault at L012C.

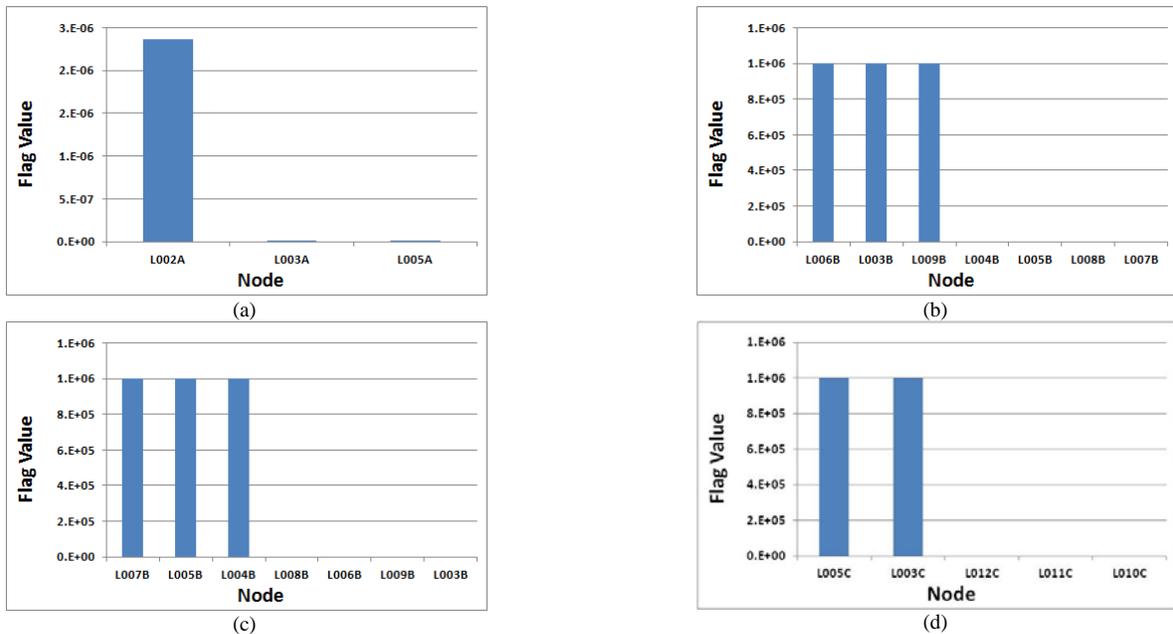


Figure 6. Results of cases, meters at half nodes: (a) Case 1: fault at L002A (b) Case 2: fault at L003B (c) Case 3: fault at L007B (d) Case 4: fault at L012C.